POLITECNICO DI TORINO
ESAMI DI STATO PER L'ABILITAZIONE ALLA PROFESSIONE
DI INGEGNERE DELL'INFORMAZIONE

I Sessione 2012 - Sezione A

Settore dell'Informazione

Classe 32/S – Ingegneria Elettronica

Prova pratica del 20 luglio 2012

Il candidato progetti un sistema elettronico per realizzare timelapse (filmati a basso frame rate, e.g. un frame ogni qualche secondo, con frame rate massimo di 1fps) e salvarli su scheda SD.

Il sistema dispone di una scheda di acquisizione, costituita da un sensore Micron MT9M001 (vedi datasheet allegato), controllato da una FPGA, e collegato mediante una opportuna connessione seriale ad una scheda di elaborazione, realizzata mediante un sistema a microprocessore.

Il sensore deve essere configurato in modalità snapshot in modo da acquisire una immagine alla volta, sempre con lo stesso tempo di esposizione deciso all'inizio del timelapse, sotto il controllo della FPGA. I dati raccolti alla risoluzione di 1280 x 1024, con dinamica ridotta agli 8 bit più significativi, devono essere decimati all'interno della FPGA in modo da ridurre la risoluzione a 320 x 240 (QVGA), dove ogni pixel dell'immagine risultante è ottenuto dalla media aritmetica di 16 pixel (4x4) dell'immagine originale. Le ultime righe dell'immagine iniziale siano ignorate.

Le immagini ottenute vengono trasmesse ad un microprocessore mediante una connessione seriale (possibilmente sincrona) e qui elaborate per realizzare un filmato in un formato standard a scelta. Il risultato dell'elaborazione viene quindi man mano salvato su una scheda SD.

Il sistema deve inoltre disporre di un tasto di start, uno di stop, un pulsante di selezione del frame rate tra un certo numero di scelte standard, e un pulsante di selezione del tempo di esposizione per ogni frame in un insieme di valori predefiniti. Dispone inoltre di un display LCD di 16 caratteri come interfaccia con l'utente. Il sistema funziona collegato alla rete elettrica a 230V, 50Hz.

In particolare si richiede:

1. Lo schema a blocchi del sistema.

2. Specifiche di dettaglio dei blocchi, con la scelta dei componenti motivata, ove possibile.

3. La configurazione dei registri del sensore per almeno due tempi di esposizione diversi, con esempi di programmazione (timing diagram) tramite l'interfaccia seriale a 2 fili.

4. Lo schema a blocchi dettagliato dell'hardware digitale contenuto all'interno della FPGA (datapath e diagramma degli stati di eventuali FSM).

5. Il flowchart (o altro schema equivalente) del codice presente sul microprocessore.

Si dettagli quindi uno a scelta tra:

- Schema elettrico della scheda di acquisizione

- Codice VHDL per le parti principali della FPGA

1/2-INCH 1.3 MEGAPIXEL CMOS ACTIVE-PIXEL DIGITAL IMAGE SENSOR

MT9M001

Micron Part Number: MT9M001C12ST

Features

- Array Format (5:4): 1,280H x 1,024V (1,310,720 active pixels). Total (incl. dark pixels): 1,312H x 1,048V (1,374,976 pixels)
- Pixel Size and Type: 5.2µm x 5.2µm active-pixel photodiode-type
- Color Filter Array: RGB Bayer primary color filters
- Optical Format: 1/2-inch
- Supply Voltage: 3.0V to 3.6V, 3.3V nominal
- Frame Rate: 30 fps progressive scan; programmable
- Data Rate: 48 MHz at 48 MHz master clock
- Responsivity (green pixels): 1.8 V/lux-sec with source illumination at 550nm
- SNR_{max}: 45dB
- Dynamic Range: 61dB
- Shutter: Electronic rolling shutter (ERS)
- Window Size: SXGA; programmable to any smaller format (VGA, QVGA, CIF, QCIF, etc.)
- Programmable Controls: Gain, frame rate, frame size
- ADC: On-chip, 10 bit
- Power Consumption:
  - Nominal: 325mW at maximum data rate (3.3V)
  - Standby: 275µW
- Operating Temperature: 0°C to +70°C
- Package: 48-pin CLCC
- Dark Current at 25°C: 20 elec/sec
- Q. E. (green): 52%
- Temporal Noise: 10e
- Saturation Voltage: 1.2V
- Pixel Capacity: 40Ke
- Conversion Gain: 32 uV/e
- Monochrome:
  - Q.E.: 56%
  - Dynamic Range: 68.2dB
  - Responsivity: 2.1 V/lux-sec

Description

The Micron® Imaging MT9M001 is an SXGA-format with a 1/2-inch CMOS active-pixel digital image sensor. The active imaging pixel array of 1,280H x 1,024V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs an SXGA-size image at 30 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

Figure 1: 48-Pin CLCC

Top pins (left to right): NC(6), DGND(5), VDD(4), NC(3), NC(2), VAA_PIX(1), AGND(48), AGND(47), SCLK(46), SDATA(45), NC(44), SCAN_EN(43)

Left pins (top to bottom): STANDBY(7), TRIGGER(8), NC(9), RESET_BAR(10), NC(11), NC(12), OE_BAR(13), NC(14), AGND(15), VAA(16), AGND(17), AGND(18)

Right pins (top to bottom): NC(42), FRAME_VALID(41), LINE_VALID(40), STROBE(39), DGND(38), VDD(37), DOUT<9>(36), DOUT<8>(35), DOUT<7>(34), DOUT<6>(33), DOUT<5>(32), PIX_CLK(31)

Bottom pins (left to right): NC(19), VAA(20), AGND(21), VDD(22), DGND(23), DOUT<0>(24), DOUT<1>(25), DOUT<2>(26), DOUT<3>(27), DOUT<4>(28), CLK_IN(29), NC(30)

Figure 2: Block Diagram

Active Pixel Sensor Array; Control Reg.; Timing And Control; 2-wire Serial Host I/F; Clock; Sync signals; Analog Processing; ADC; 10-bit Data; MI-1300
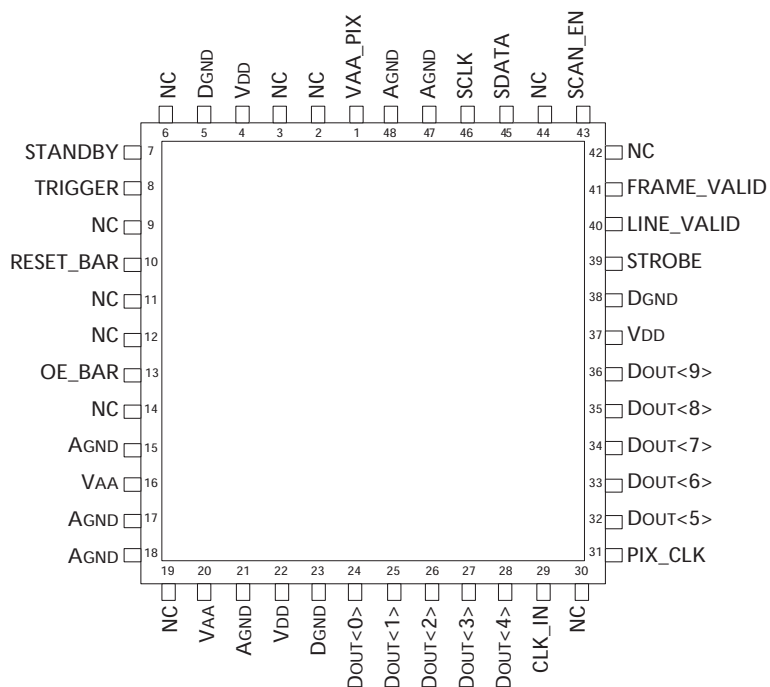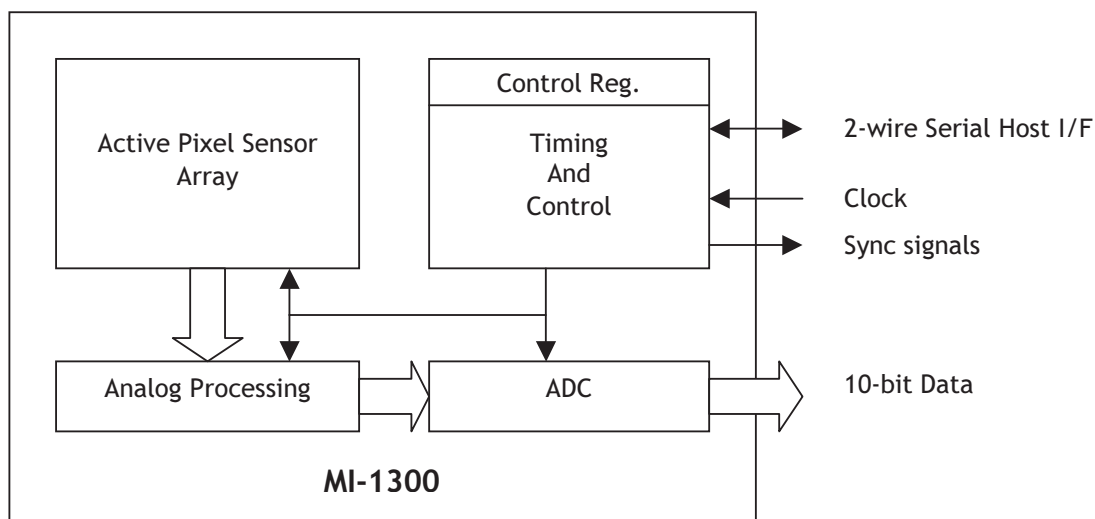
Table 1: Pin Descriptions

| PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
29	CLK_IN	Input	Clock In: Master clock into sensor (48 MHz maximum).
13	OE_BAR	Input	Output Enable: OE_BAR when HIGH places outputs D_{OUT}<0–9>, FRAME_VALID, LINE_VALID, PIX_CLK, and STROBE into a tri-state configuration.
10	RESET_BAR	Input	Reset: Activates (LOW) asynchronous reset of sensor. All registers assume factory defaults.
46	SCLK	Input	Serial Clock: Clock for serial interface.
7	STANDBY	Input	Standby: Activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
8	TRIGGER	Input	Trigger: Activates (HIGH) snapshot sequence.
43	SCAN_EN	Input	Tie to digital ground.
45	SDATA	Input/Output	Serial Data: Serial data bus, requires 1.5KΩ resistor to 3.3V for pull-up.
24–28, 32–36	D_{OUT}<0–9>	Output	Data Out: Pixel data output bits 0–9, D_{OUT}<9> (MSB), D_{OUT}<0> (LSB).
41	FRAME_VALID	Output	Frame Valid: Output is pulsed HIGH during frame of valid pixel data.
40	LINE_VALID	Output	Line Valid: Output is pulsed HIGH during line of selectable valid pixel data (see Reg0x20 for options).
31	PIX_CLK	Output	Pixel Clock: Pixel data outputs are valid during falling edge of this clock. Frequency = (master clock).
39	STROBE	Output	Strobe: Output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
15, 17, 18, 21, 47, 48	A_{GND}	Supply	Analog Ground: Provide isolated ground for analog block and pixel array.
5, 23, 38	D_{GND}	Supply	Digital Ground: Provide isolated ground for digital block.
16, 20	VAA	Supply	Analog Power: Provide power supply for analog block, 3.3V ±0.3V.
1	VAA_PIX	Supply	Analog Pixel Power: Provide power supply for pixel array, 3.3V ±0.3V (3.3V).
4, 22, 37	VDD	Supply	Digital Power: Provide power supply for digital block, 3.3V ±0.3V.
2, 3, 6, 9, 11, 12, 14, 19, 30, 42, 44	NC	–	No Connect: These pins must be left unconnected.

Pixel Data Format

Pixel Array Structure

The MT9M001 pixel array is configured as 1,312 columns by 1,048 rows (shown in Figure 3). The first 16 columns and the first eight rows of pixels are optically black, and can be used to monitor the black level. The last seven columns and the last seven rows of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. However, the black rows can also be read out by setting the sensor to raw data output mode (Reg0x20, bit 11 = 1). There are 1,289 columns by 1,033 rows of optically active pixels, which provides a four-pixel boundary around the SXGA (1,280 x 1,024) image to avoid boundary effects during color interpolation and correction.

Figure 3: Pixel Array Description
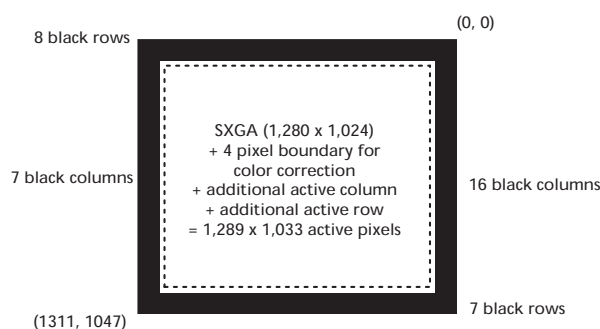
The MT9M001 uses a Bayer color pattern, as shown in Figure 4. The even-numbered rows contain green and red color pixels, and odd numbered rows contain blue and green color pixels. Likewise, the even numbered columns contain green and blue color pixels, and odd numbered columns contain red and green color pixels.

Figure 4: Pixel Color Pattern Detail (Top Right Corner)
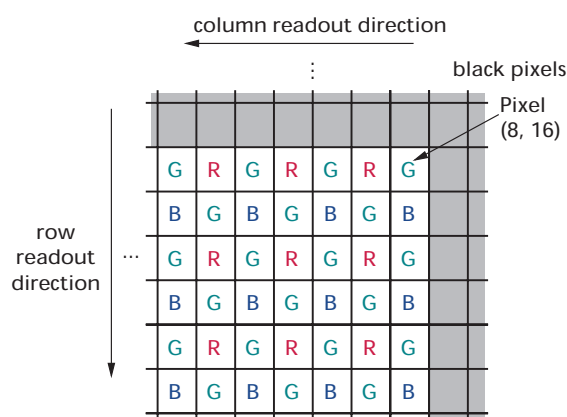
Output Data Format

The MT9M001 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 5. The amount of horizontal blanking and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in the next section.

Figure 5: Spatial Illustration of Image Readout

$P_{0,0}$ $P_{0,1}$ $P_{0,2}$................................$P_{0,n-1}$ $P_{0,n}$ $P_{1,0}$ $P_{1,1}$ $P_{1,2}$................................$P_{1,n-1}$ $P_{1,n}$ VALID IMAGE $P_{m-1,0}$ $P_{m-1,1}$·····································$P_{m-1,n-1}$ $P_{m-1,n}$ $P_{m,0}$ $P_{m,1}$·····································$P_{m,n-1}$ $P_{m,n}$	00 00 00 .... 00 00 00 00 00 00 .... 00 00 00 HORIZONTAL BLANKING 00 00 00 .... 00 00 00 00 00 00 .... 00 00 00
00 00 00 .... 00 00 00 00 00 00 .... 00 00 00 VERTICAL BLANKING 00 00 00 .... 00 00 00 00 00 00 .... 00 00 00	00 00 00 .... 00 00 00 00 00 00 .... 00 00 00 VERTICAL/HORIZONTAL BLANKING 00 00 00 .... 00 00 00 00 00 00 .... 00 00 00

Output Data Timing

The data output of the MT9M001 is synchronized with the PIX_CLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIX_CLK period.

Figure 6: Timing Example of Pixel Data
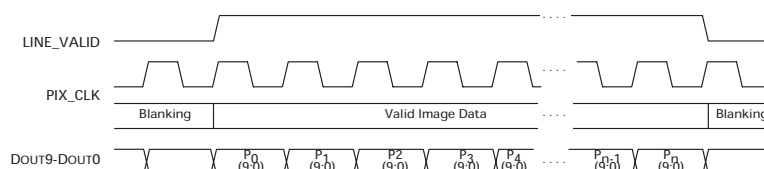
The rising edges of the PIX_CLK signal are nominally timed to occur on the rising DOUT edges. This allows PIX_CLK to be used as a clock to latch the data. DOUT data is valid on the falling edge of PIX_CLK. The PIX_CLK is HIGH while master clock is HIGH and then LOW while master clock is LOW. It is continuously enabled, even during the blanking period.

Figure 7: Row Timing and FRAME_VALID/LINE_VALID Signals
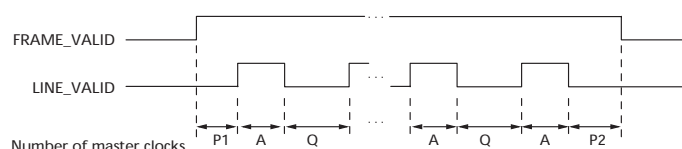
Frame Timing Formulas
Table 2:   Frame Timing

PARAMETER	NAME	EQUATION (MASTER CLOCK)	DEFAULT TIMING	NOTES
A	Active Data Time	(Reg0x04 + 1)	1,280 pixel clocks $= 26.7\mu s$	1
P_1	Frame Start Blanking	(242)	242 pixel clocks $= 5.04\mu s$	
P_2	Frame End Blanking	(2 + Reg0x05 - 19) (MIN Reg0x05 value = 19)	2 pixel clocks $= 0.042\mu s$	2
$Q = P_1 + P_2$	Horizontal Blanking	(244 + Reg0x05 - 19) (MIN Reg0x05 value = 19)	244 pixel clocks $= 5.08\mu s$	2
A + Q	Row Time	((Reg0x04 + 1) + (244 + Reg0x05 - 19))	1,524 pixel clocks $= 31.75\mu s$	
V	Vertical Blanking	(Reg0x06 + 1) x (A + Q) (MIN Reg0x06 value = 15)	39,624 pixel clocks $= 825.5\mu s$	
N_{rows} x (A + Q)	Frame Valid Time	(Reg0x03 + 1) x (A + Q)	1,560,576 pixel clocks $= 32.51ms$	
F	Total Frame Time	(Reg0x03 + 1 + Reg0x06 + 1) x (A + Q)	1,600,200 pixel clocks $= 33.34ms$	

NOTE:

1. Row skip mode should have no effect on the integration time. Column skip mode changes the effective value of Column Size (Reg0x04) as follows:
   Column Skip 2 => R4eff = (int(R4 / 4) x 2) + 1
   Column Skip 4 => R4eff = (int(R4 / 8) x 2) + 1
   Column Skip 8 => R4eff = (int(R4 / 16) x 2) + 1
   where the int() function truncates to the next lowest integer. Now use R4eff in the equation for row time instead of R4
2. Default for Reg0x05 = 9. However, sensor ignores any value for Reg0x05 less than 19.

Sensor timing is shown above in terms of pixel clock and master clock cycles (please refer to Figure 6). The recommended master clock frequency is 48 MHz. The vertical blank and total frame time equations assume that the number of integration rows (bits 13 through 0 of Reg0x09) is less than the number of active plus blanking rows (Reg0x03 + 1 + Reg0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 3.

Table 3:   Frame Time – Long Integration Time

PARAMETER	NAME	EQUATION (MASTER CLOCK)	DEFAULT TIMING
V′	Vertical Blanking (long integration time)	(Reg0x09 – Reg0x03) x (A + Q)	39,624 pixel clocks $= 82.5\mu s$
F′	Total Frame Time (long integration time)	(Reg0x09 + 1) x (A + Q)	1,600,200 pixel clocks $= 33.34ms$

Serial Bus Description

Registers are written to and read from the MT9M001 through the two-wire serial interface bus. The sensor is a two-wire serial interface slave and is controlled by the two-wire serial interface clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out through the MT9M001 two-wire serial interface data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the two-wire serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial interface bus defines several different transmission codes, as follows:
- a start bit
- the slave device eight-bit address
- a(an) (no) acknowledge bit
- an eight-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's eight-bit address. The last bit of the address determines if the request will be a read or a write, where a "0" indicates a write and a "1" indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the eight-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9M001 uses 16-bit data for its internal registers, thus requiring two eight-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and eight-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowl-

edge bit after each eight-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The eight-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A "0" in the LSB (least significant bit) of the address indicates write mode, and a "1" indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 8. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit transfer, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

Figure 8: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284
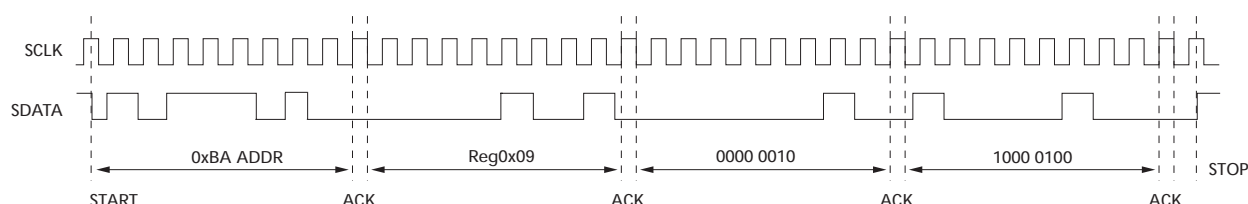

16-Bit Read Sequence

A typical read sequence is shown in Figure 9. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 9: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284
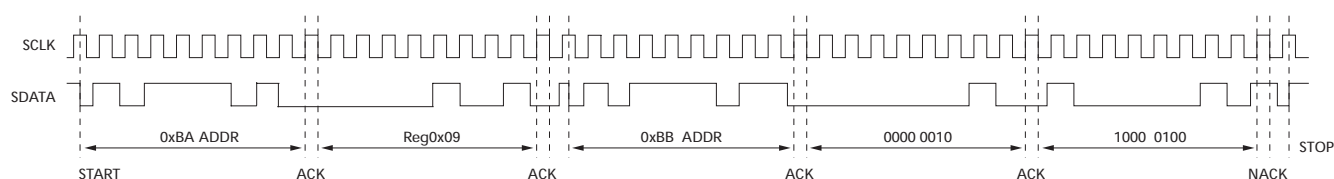
Registers

Register Map

Table 4:   Register List and Default Values
Note 1

REGISTER # (HEX)	DESCRIPTION	DATA FORMAT (BINARY)	DEFAULT VALUE (HEX)	NOTES
0x00	Chip Version	1000 0100 0001 0001	0x8421	2
0x01	Row Start	0000 0ddd dddd dddd	0x000C	
0x02	Column Start	0000 0ddd dddd dddd	0x0014	
0x03	Row Size (Window Height)	0000 0ddd dddd dddd	0x03FF	
0x04	Col Size (Window Width)	0000 0ddd dddd dddd	0x04FF	
0x05	Horizontal Blanking	0000 0ddd dddd dddd	0x0009	
0x06	Vertical Blanking	0000 0ddd dddd dddd	0x0019	
0x07	Output Control	0000 0000 0d00 00dd	0x0002	
0x09	Shutter Width	00dd dddd dddd dddd	0x0419	
0x0B	Restart	0000 0000 0000 000d	0x0000	
0x0C	Shutter Delay	0000 0ddd dddd dddd	0x0000	
0x0D	Reset	0000 0000 0000 000d	0x0000	
0x1E	Read Options 1	1000 dddd 00dd dd00	0x8000	
0x20	Read Options 2	dd01 0dd1 d00d d10d	0x1104	
0x2B	Green1 Gain	0000 0000 0ddd dddd	0x0008	
0x2C	Blue Gain	0000 0000 0ddd dddd	0x0008	
0x2D	Red Gain	0000 0000 0ddd dddd	0x0008	
0x2E	Green2 Gain	0000 0000 0ddd dddd	0x0008	
0x35	Global Gain	0000 0000 0ddd dddd	0x0008	
0x5F	Cal Threshold	dddd dddd d0dd dddd	0x0904	
0x60	Cal Green1	0000 000d dddd dddd	0x0000	3
0x61	Cal Green2	0000 000d dddd dddd	0x0000	3
0x62	Cal Ctrl	d00d d100 1001 1ddd	0x0498	
0x63	Cal Red	0000 000d dddd dddd	0x0000	3
0x64	Cal Blue	0000 000d dddd dddd	0x0000	3
0xF1	Chip Enable	0000 0000 0000 00dd	0x0001	

NOTE:

1. 1 = always 1
    0 = always 0
    d = programmable
2. Previous version used the data format of 1000 0100 0001 0001; hex value of 0x8411.
3. In default mode, calibration values start at "0" but are set via dark level calibration.

Table 5: Register Description

REGISTER	BIT	DESCRIPTION
Chip ID		
0x00	0–15	This register is read-only and gives the chip identification number: 0x8421.
Window Control		
These registers control the size of the window.		
0x01	0–10	First row to be read out—default = 0x000C (12).
0x02	0–10	First column to be read out—default = 0x0014 (20). Register value must be an even number.
0x03	0–10	Window height (number of rows - 1)—default = 0x03FF (1023). Minimum value for 0x03 = 0x0002.
0x04	0–10	Window width (number of columns - 1)—default = 0x04FF (1279). Register value must be an odd number. Minumum value for 0x04 = 0x0003.
Blanking Control		
These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using Table 2, Frame Timing, on page 6.		
0x05	0–10	Horizontal Blanking—default = 0x0009 (9 pixels).
0x06	0–10	Vertical Blanking—default = 0x0019 (25 rows).
Output Control		
This register controls various features of the output format for the sensor.		
0x07	0	Synchronize changes (copied to Reg0xF1, bit1). 0 = normal operation. Update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip or row mirror) at the next frame boundary. The "frame boundary" is 8 row_times before the rising edge of FRAME_VALID. (If "Show Dark Rows" is set, it will be coincident with the rising edge of FRAME_VALID.) 1 = do not update any changes to these settings until this bit is returned to "0."
	1	Chip Enable (copied to Reg0xF1, bit0). 1 = normal operation. 0 = stop sensor readout. When this is returned to "1," sensor readout restarts at the starting row in a new frame. The digital power consumption can then also be reduced to less than 5uA by turning off the master clock.
	2	Reserved—default is 0; set to zero at all times.
	3	Reserved—default is 0; set to zero at all times.
	6	Override pixel data. 0 = normal operation. 1 = output programmed test data (see Reg0x32). First valid columns will output contents of test data register; second columns will output inverted data. Third columns will output noninverted data, fourth inverted, etc.

Table 5: Register Description (continued)

REGISTER	BIT	DESCRIPTION
Pixel Integration Control		
These registers (along with the window sizing and blanking registers) control the integration time for the pixels. The actual total integration time (^{t}INT) is: ^{t}INT = Reg0x09 x row time - overhead time - reset delay, where: Row time = ((Reg0x04 + 1) + 244 + Reg0x05 - 19) pixel clock periods Overhead time = 180 pixel clock periods Reset delay = 4 x Reg0x0C pixel clock periods If the value in Reg0x0C exceeds (row time - 548)/4 pixel clock cycles, the row time will be extended by (4 x Reg0x0C - (row time - 548)) pixel clock cycles. In this expression, the row time term, Reg0x09 x ((number of columns) + 244 + horizontal blanking register - 19), corresponds to the number of rows integrated. The overhead time (180 pixel clocks) is the overhead time between the READ cycle and the RESET cycle, and the final term is the effect of the reset delay. Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows) such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the MT9M001 will add additional blanking rows as needed. A second constraint is that ^{t}INT must be adjusted to avoid banding in the image from light flicker. Under 60Hz flicker, this means ^{t}INT must be a multiple of 1/120 of a second. Under 50Hz flicker, ^{t}INT must be a multiple of 1/100 of a second.		
0x09	0–13	Number of rows of integration—default = 0x0419 (1049).
0x0C	0–10	Shutter delay—default = 0x0000 (0). This is the number of master clocks times four that the timing and control logic waits before asserting the reset for a given row.
Frame Restart		
0x0B	0	Setting bit 0 to "1" of Reg0x0B will cause the sensor to abandon the readout of the current frame and restart from the first row. This register automatically resets itself to 0x0000 after the frame restart. The first frame after this event is considered to be a "bad frame" (see description for Reg0x20, bit0).
Reset		
0x0D	0	This register is used to reset the sensor to its default, power-up state. To put the MT9M001 in reset mode first write a "1" into bit 0 of this register, then write a "0" into bit 0 to resume operation.
Read Mode 1		
In read mode 1, this register is used to control many aspects of the readout of the sensor.		

Table 5:   Register Description (continued)

REGISTER	BIT	DESCRIPTION
0x1E	0	Reserved—default is 0; set to zero at all times.
	1	Reserved—default is 0; set to zero at all times.
	2	Column Skip 4—default is 0 (disable). 1 = enable.
	3	Row Skip 4—default is 0 (disable). 1 = enable.
	4	Column Skip 8—default is 0 (disable). 1 = enable.
	5	Row Skip 8—default is 0 (disable). 1 = enable.
	6	Reserved—default is 0; do not change.
	7	Reserved—default is 0; do not change.
	8	Snapshot Mode—default is 0 (continuous mode). 1 = enable (wait for TRIGGER; TRIGGER can come from outside signal (TRIGGER pin on the sensor) or from serial interface register restart, i.e. programming a "1" to bit 0 of Reg0x0B.
	9	STROBE Enable—default is 0 (no STROBE signal). 1 = enable STROBE (signal output from the sensor during the time all rows are integrating. See STROBE width for more information).
	10	STROBE Width—default is 0 (STROBE signal width at minimum length, 1 row of integration time, prior to line valid going HIGH). 1 = extend STROBE width (STROBE signal width extends to entire time all rows are integrating).
0x1E	11	Strobe Override—default is 0 (STROBE signal created by digital logic). 1 = override STROBE signal (STROBE signal is set HIGH when this bit is set, LOW when this bit is set LOW. It is assumed that STROBE enable is set to "0" if STROBE override is being used).
	12	Reserved—default is 0; do not change.
	13	Reserved—default is 0; do not change.
	14	Reserved—default is 0; do not change.
	15	Reserved—default is 1; do not change.
Read Mode 2 This register is used to control many aspects of the readout of the sensor.		

Table 5: Register Description (continued)

REGISTER	BIT	DESCRIPTION
0x20	0	No bad frames—1 = output all frames (including bad frames). 0 (default) = only output good frames. A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, row or column skip, or mirroring.
	1	Reserved—default is 0; do not change.
	2	Reserved—default is 1; set to "1" at all times.
	3	Column skip—1= read out two columns, and then skip two columns (for example, col 0, col 1, col 4, col 5…). 0 = normal readout (default).
	4	Row skip—1 = read out two rows, and then skip two rows (for example, row 0, row 1, row 4, row 5…). 0 = normal readout (default).
	5	Reserved—default is 0; do not change.
	6	Reserved—default is 0; set to zero at all times.
	7	Flip Row—1 = readout starting 1 row later (alternate color pair). 0 (default) = normal readout.
	8	Reserved—default is 1; set to "1" at all times.
	9	1 = "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blanking). 0 = normal LINE_VALID (default, no LINE_VALID during vertical blanking).
	10	1 = LINE_VALID = "Continuous" LINE_VALID XOR FRAME_VALID. 0 = LINE_VALID determined by bit 9.
	11	Reserved—default is 0; do not change.
	12	Reserved—default is 1; do not change.
	13	Reserved—default is 0; do not change.
	14	Reserved—default is 0; do not change.
	15	Mirror Row—1 = read out from bottom to top (upside down). 0 (default) = normal readout (top to bottom).

Gain Settings
The gain is individually controllable for each color in the Bayer pattern as shown in the register chart.

Formula for gain setting:
Gain ≤ 8
$$\text{Gain} = (\text{bit}[6] + 1) \times (\text{bit}[5\text{-}0] \times 0.125)$$
Gain > 8 (bit[6] = 1 and bit[5] = 1)
$$\text{Gain} = 8.0 + \text{bit}[2\text{-}0]$$

Since bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. The following lists the recommended gain settings:

Gain	Increments	Recommended Settings
1.000 to 4.000	0.125	0x08 to 0x20
4.25 to 8.00	0.25	0x51 to 0x60
9.0 to 15.0	1.0	0x61 to 0x67

0x2B	6–0	Green1 gain—default = 0x08 (8) = 1x gain.
0x2C	6–0	Blue gain—default = 0x08 (8) = 1x gain.
0x2D	6–0	Red gain—default = 0x08 (8) = 1x gain.
0x2E	6–0	Green2 gain—default = 0x08 (8) = 1x gain.

Table 5: Register Description (continued)

REGISTER	BIT	DESCRIPTION
0x35	6–0	Global gain—default = 0x08 (8) = 1x gain. This register can be used to set all four gains at once. When read, it will return the value stored in Reg0x2B.
Black level Calibration		
These registers are used in the black level calibration. Their functionality is described in detail in the next section.		
0x5F	5–0	Thres_lo—Lower threshold for black level in ADC LSBs—default = 000100.
	7	1 = override automatic Thres_hi and Thres_lo adjust (Thres_hi always = bits 14–8; Thres_lo always = bits 5–0). Default = 0 = Automatic Thres_hi and Thres_lo adjustment.
	14-8	Thres_hi—Maximum allowed black level in ADC LSBs (default = Thres_lo + 5). Black level maximum is set to this value when bit 7 = 1; black level maximum is reset to this value after every black level average restart if bit 15 = 1 and bit 7 = 0.
	15	No gain dependence. 1 = Thres_lo is set by the programmed value of bits 5–0, Thres_hi is reset to the programmed value (bits 14–8) after every black level average restart. 0 = Thres_lo and Thres_hi are set automatically, as described above.
0x60	8–0	Cal Green1—analog offset correction value for Green 1, bits 0–7 sets magnitude, bit 8 set sign. 2's complement, if bit 8 = 1, Offset = bits [0-7] - 256. 0 = positive. 1 = negative.
0x61	8–0	Cal Green2—analog offset correction value for Green 2, bits 0–7 sets magnitude, bit 8 set sign. 0 = positive. 1 = negative.
0x62	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).
0x62	2–1	Force/disable black level calibration. 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously. X1= disable black level correction (Offset Correction Voltage = 0.0V). (In this case, no black level correction is possible).
	4–3	Reserved—default is 1; do not change.
	6–5	Reserved—default is 0; do not change.
	7	Reserved—default is 1; do not change.
	9–8	Reserved—default is 0; do not change.
	10	Reserved—default is 1; do not change.
	11	1 = do not reset the upper threshold after a black level recalculation sweep. 0 = reset the upper threshold after a black level recalculation sweep (default).
	12	1 = start a new running digitally filtered average for the black level (this is internally reset to "0" immediately), and do a rapid sweep to find the new starting point. 0 = normal operation (default).
	14–3	Reserved—default is 0; set to zero at all times.
	15	1 = do not perform the rapid black level sweep on new gain settings. 0 = normal operation.
0x63	8–0	Cal Red—analog offset correction value for Red, bits 0–7 sets magnitude, bit 8 set sign. 2's complement, if bit 8 = 1, Offset = bits [0-7] - 256. 0 = positive. 1 = negative.

Table 5: Register Description (continued)

REGISTER	BIT	DESCRIPTION
0x64	8–0	Cal Blue—analog offset correction value for Blue, bits 0–7 sets magnitude, bit 8 set sign. 2's complement, if bit 8 = 1, Offset = bits [0-7] - 256. 0 = positive. 1 = negative.
Chip Enable and Two-wire serial interface write synchronize.		
0xF1	0	Mirrors the functionality of Reg0x07 bit1 (Chip Enable). 1 = normal operation. 0 = stop sensor readout; when this is returned to "1," sensor readout restarts at the starting row in a new frame.
	1	Mirrors the functionality of Reg0x07 bit0 (Synchronize changes). 0 = normal operation, update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip, or row/column mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to "0."

Feature Description

Signal Path

The MT9M001 signal path consists of two stages, a programmable gain stage and a programmable analog offset stage.

Programmable Gain Stage

The gain settings can be independently adjusted for the colors Green1, Blue, Red, and Green2 and are programmed through registers 0x2B, 0x2C, 0x2D, and 0x2E, respectively. A total programmable gain of 15 is available and can be calculated using the following formula:

Gain 1 to 8:   Gain = (bit[6] + 1) x (bit[5-0] x 0.125)

For gain higher than eight, the user would need to set bit[6-5] = 11 and use the lower 3 LSB's bit[2-0] to set the higher gain values. The formula for obtaining gain greater than eight is as follows:

Total gain = 8 + bit[2-0]

For example, for total gain = 12, the value to program is bit[6-0] = 1100100.

The maximum total gain = 15, i.e. bit[6-0] = 1100111.

The gain circuitry in the MT9M001 is designed to offer signal gains from one to 15. The minimum gain of one corresponds to the lowest setting where the pixel signal is guaranteed to saturate the ADC under all specified operating conditions. Any reduction of the gain below this value may cause the sensor to saturate at ADC output values less than the maximum, under certain conditions. It is recommended that this guideline be followed at all times.

Since bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. Recommended gain settings are listed in Table 6.
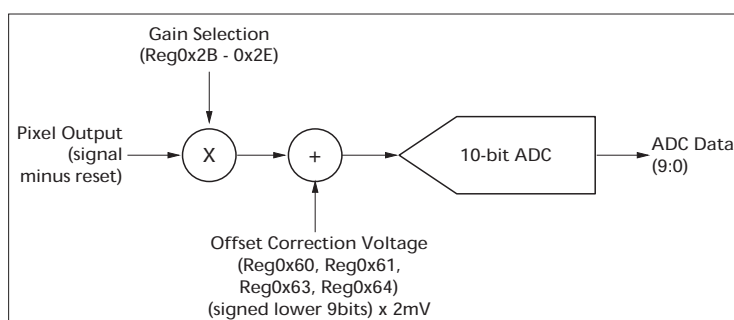
Figure 10: Signal Path

Table 6:   Recommended Gain Settings at 48 MHz

NOMINAL GAIN	INCREMENTS	RECOMMENDED SETTINGS
1 to 4.000	0.125	0x08 to 0x20
4.25 to 8.00	0.25	0x51 to 0x60
9 to 15	1.0	0x61 to 0x67

Programmable Analog Offset Stage

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The analog offset settings can be independently adjusted for the colors Green1, Green2, Red, and Blue and are programmed through registers 0x60, 0x61, 0x63, and 0x64, respectively. The user would need to program register 0x62 appropriately to enable the analog offset correction.

The lower eight bits (bit[7-0]) determines the absolute value of the analog offset to be corrected and bit[8] determines the sign of the correction. When bit[8] is "1", the sign of the correction is negative and vice versa. The analog value of the correction relative to the analog gain stage can be determined from the following formula:
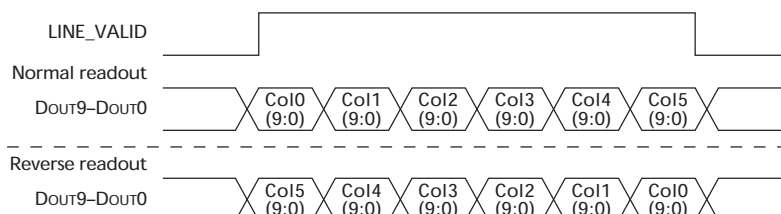
Analog offset (bit[8] = 0) = bit[7-0] x 2mV
Analog offset (bit[8] = 1) = - (bit[7-0] x 2mV)
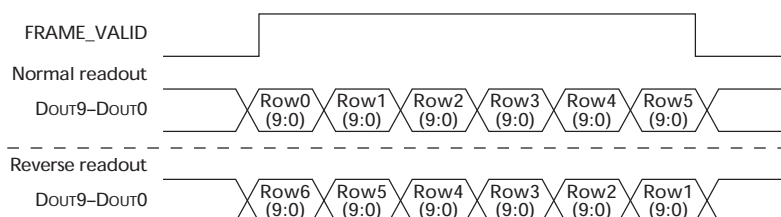
Column and Row Mirror Image

By setting bit 14 of Reg0x20, the readout order of the columns will be reversed, as shown in Figure 11.

**Figure 11: Readout of Six Columns in Normal and Column Mirror Output Mode**

By setting bits 15 of Reg0x20 the readout order of the rows will be reversed, as shown in Figure 12.

Figure 12: Readout of Six Rows in Normal and Row Mirror Output Mode

By setting bits 15 and 7 of Reg0x20 the readout order of the rows will be reversed and maintain color order as shown in the figure below.

Figure 13: Readout of Six Rows in Normal and Row Mirror Output Mode with Color Order Maintained
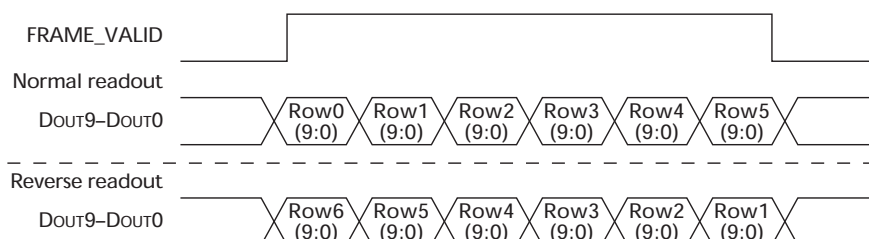
Column and Row Skip

By setting bit 3 of Reg0x20, only half of the columns set will be read out. An example is shown in Figure 14. Only columns with bit 1 equal to "0" will be read out (xxxxxxx0x). The row skip works in the same way and will only read out rows with bit 1 equal to "0." Row skip mode is enabled by setting bit 4 of Reg0x20. For both row and column skips, the number of rows or columns read out will be half of what is set in Reg0x03 or Reg0x04, respectively.

Figure 14: Readout of Eight Pixels in Normal and Column Skip Output Mode
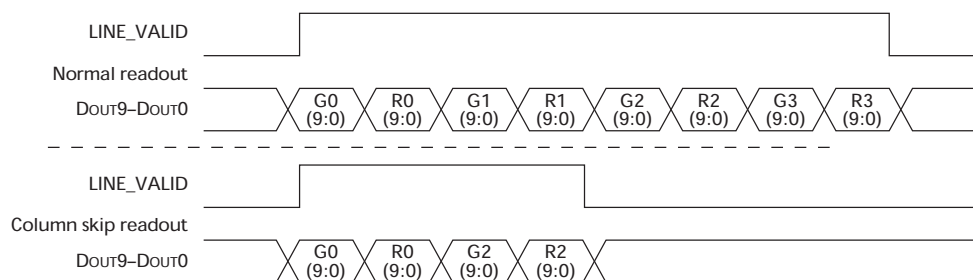
Still Image Capture with External Synchronization

In continuous mode video image capture, the TRIGGER signal should be held LOW or "0." To capture a still image, the sensor must first be put into snapshot mode by programming a "1" in register 0x1E, bit 8. In snapshot mode, the sensor waits for a TRIGGER signal (FRAME_VALID, LINE_VALID signals are LOW, pixel clock signal continues). When the TRIGGER signal is received (active HIGH), one frame is read out (a TRIGGER signal can also be achieved by programming a restart—for example, program a "1" to bit 0 of Reg0x0B). The reset, readout timing for that frame will be the same as for a continuous frame with similar register settings; the only difference is that only one frame is read out. General timing for the snapshot mode is shown in Figure 16.

**Figure 16: General Timing for Snapshot Mode**
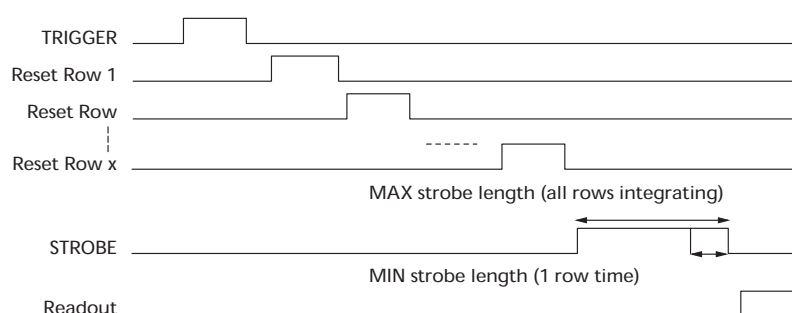
LINE_VALID Signal

By setting bit 9 and 10 of Reg0x20 the line valid signal can get three different output formats. The formats are shown when reading out four rows and two vertical blanking rows (Figure 17). In the last format, the LINE_VALID signal is the XOR between the continuously LINE_VALID signal and the FRAME_VALID signal.

Figure 17: Different LINE_VALID Formats
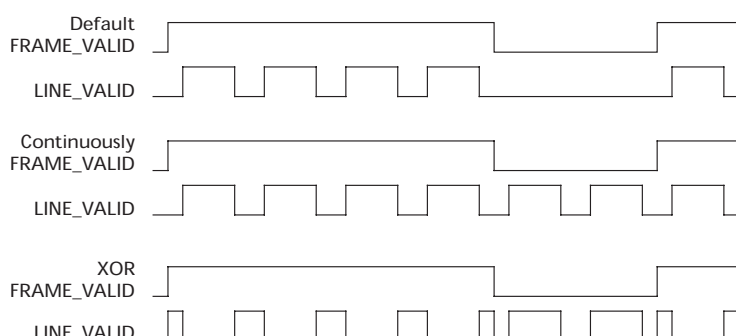
Electrical Specifications

Table 8: DC Electrical Characteristics

(V_{PWR} = 3.3 ±0.3V; T_A = 25°C)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage		V_{PWR} - 0.3	3.3	V_{PWR} + 0.3	V	
V_{IL}	Input Low Voltage		-0.3	0.0	0.8	V	
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{PWR} or V_{GND}	-15	0.8	15	µA	
V_{OH}	Output High Voltage		V_{PWR} - 0.2	3.3		V	
V_{OL}	Output Low Voltage			0.0	0.2	V	
I_{OZ}	Tri-state Output Leakage Current				15	µA	
I_{PWRA}	Analog Quiescent Supply Current	Default settings	50	85	110	mA	
I_{PWRD}	Digital Quiescent Supply Current	CLK_IN = 48 MHz; default setting, C_{LOAD} = 10pF	16	20	24	mA	
I_{PWRA} Standby	Analog Standby Supply Current	STDBY = V_{DD}	--	80	100	µA	1
I_{PWRD} Standby	Digital Standby Supply Current	STDBY = V_{DD}, CLK_IN = 0 MHz	--	9	20	µA	1
I_{PWRD} Standby ClkOn	Digital Standby Supply Current with Clock On	STDBY = V_{DD}, CLK_IN = 48 MHz	--	55	125	µA	

NOTE:

1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.

Table 9: AC Electrical Characteristics

(V_{PWR} = 3.3 ±0.3V; T_A = 25°C; CLK_IN at 48 MHz)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNITS
FCLK_IN	Input Clock Frequency Clock		1		48	MHz
	Duty Cycle		45/55	50/50	55/45	MIN/MAX ns
t_R	InputClock Rise Time		TBD	TBD	TBD	ns
t_F	Input Clock Fall Time		TBD	TBD		ns
t_{PLHP}	CLK_IN to PIX_CLK propagation delay, LOW-to-HIGH	C_{LOAD} = 10pF	--	11.5	--	ns
t_{PHLP}	CLK_IN to PIX_CLK propagation delay, HIGH-to-LOW	C_{LOAD} = 10pF		11.5		ns
t_{PHLD}	CLK_IN to D_{OUT}<9-0> propagation delay, LOW-to-HIGH	C_{LOAD} = 10pF		13.5		ns
t_{PHLD}	CLK_IN to D_{OUT}<9-0> propagation delay, HIGH-to-LOW	C_{LOAD} = 10pF		13.5		ns
t_{OH}	Data Hold Time			13.1		ns
$t_{PLHF,L}$	CLK_IN to FRAME_VALID and LINE_VALID propagation, LOW-to-HIGH	C_{LOAD} = 10pF		TBD		ns
$t_{PHLF,L}$	CLK_IN to FRAME_VALID and LINE_VALID propagation, HIGH-to-LOW			TBD		ns