POLITECNICO DI TORINO
ESAMI DI STATO PER L'ABILITAZIONE ALLA PROFESSIONE
DI INGEGNERE DELL'INFORMAZIONE

I Sessione 2016 - Sezione A
Settore dell'Informazione

PROVA PRATICA del 22 luglio 2016

Il candidato svolga uno a scelta fra i seguenti temi proposti.
Gli elaborati prodotti dovranno essere stilati in forma chiara e ordinata.
La completezza, l'attinenza e la chiarezza espositiva costituiranno elementi di valutazione.

Tema n. 1

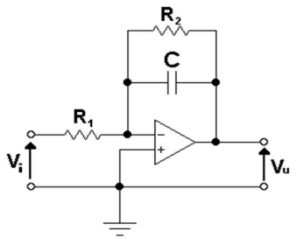
a) Disegnare lo schema a blocchi di un defibrillatore cardioversore esterno descrivendo le funzioni ed i principali parametri che caratterizzano ogni blocco.
b) Considerato che il dispositivo deve essere in grado di erogare shock da 10J a 350J dimensionare il condensatore e riportare la tensione minima e massima alla quale deve essere caricato, commentando in modo dettagliato le scelte eseguite.
c) Sapendo che due scariche successive devono poter essere erogate dieci secondi una dopo l'altra, descrivere le principali caratteristiche del circuito di carica del condensatore con particolare attenzione alla modalità di carica, alla potenza massima ed alla massima corrente che deve essere in grado di erogare.
d) Dimensionare e descrivere lo schema funzionale e le caratteristiche dei singoli blocchi (fisici o computazionali) del circuito di misura dell'energia immagazzinata e di quella ceduta al paziente.
e) Predisporre un programma di manutenzione preventiva per generici defibrillatori cardioversori esterni, distinguendo tra interventi e verifiche eseguibili dall'operatore sanitario (primo livello) ed interventi e verifiche eseguibili dal personale del servizio di ingegneria clinica (secondo livello). Si elenchino tutti gli strumenti che dovranno essere disponibili all'interno del servizio di ingegneria clinica per effettuare le verifiche necessarie, le istruzioni dettagliate per ogni verifica e si indichino, dove appropriato, gli intervalli di validità del valore delle variabili misurate e la frequenza con la quale eseguire le misure.

Tema n. 2

Il candidato progetti un controllo per un simulatore analogico di processo.

Prima parte

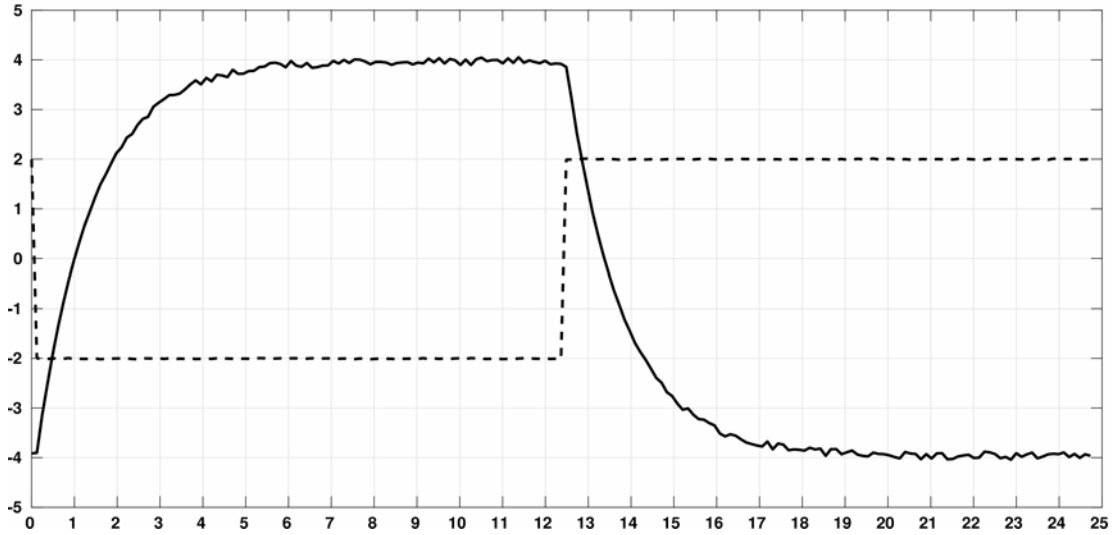
A) In base alla figura seguente



il candidato ricavi un modello fisico del dispositivo elettronico, supponendo l'amplificatore operazionale ideale e i seguenti valori numerici dei parametri:

$$R_1 = 1\,\mathrm{M}\Omega, \quad R_2 = 2\,\mathrm{M}\Omega, \quad C = 680\,\mathrm{nF}$$

B) Il candidato identifichi un modello dinamico lineare sulla base della risposta al gradino rappresentata in figura, dove la linea tratteggiata rappresenta la variazione della tensione d'ingresso V_i in volt e la linea continua rappresenta la conseguente variazione della tensione d'uscita V_u in volt.



Il candidato scelga l'ordine del modello in modo che sia minimo, pur riproducendo ragionevolmente bene l'andamento dell'uscita, e ne ricavi i valori numerici dei parametri argomentando le scelte fatte.

C) Il candidato confronti i risultati ottenuti al punto A e al punto B.

Seconda parte

Si ipotizzi che l'impianto fisico sia modellabile da due simulatori di processo come descritti nella *Prima parte* posti in cascata. Di conseguenza, a prescindere dai risultati ottenuti nella *Prima parte*, si assuma come modello complessivo dell'impianto la seguente funzione di trasferimento:

$$\frac{V_u(s)}{V_i(s)} = \frac{4}{(1+1.36\,s)^2}$$

Il committente richiede il progetto di un dispositivo di controllo che soddisfi i seguenti due requisiti:

1 – la tensione d'uscita a regime deve essere esattamente uguale alla tensione di riferimento supposta costante;

2 – la tensione d'uscita deve raggiungere la tensione di riferimento, senza superarla, in circa 2 secondi.

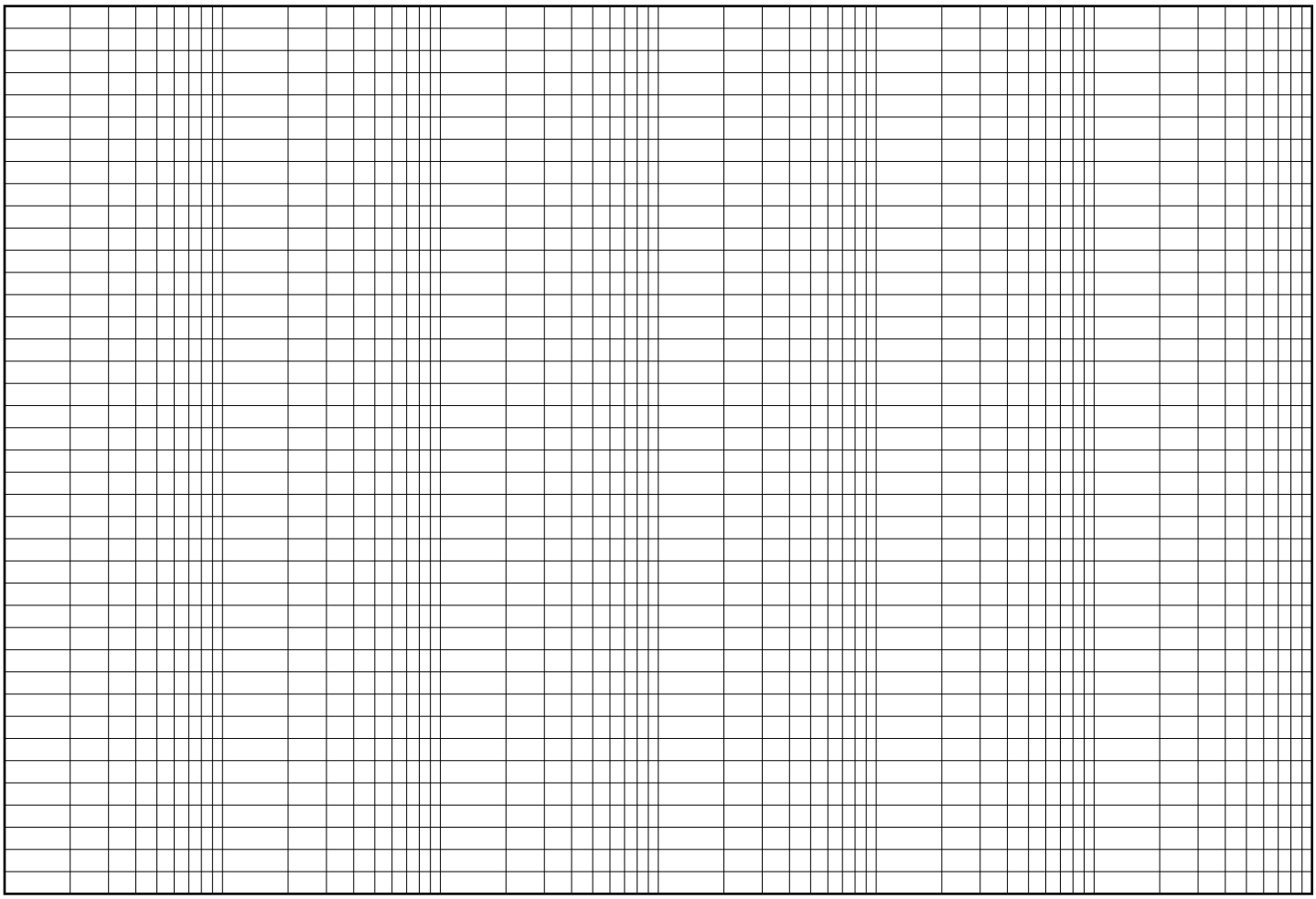
Il candidato trasformi questi due requisiti qualitativi in specifiche (come intese abitualmente in ambito controllistico), ed eventualmente ne aggiunga altre ritenute necessarie.

Quindi, sulla base delle specifiche da lui definite e del modello complessivo dell'impianto, progetti un dispositivo di controllo digitale, caratterizzandone la struttura e l'algoritmo; inoltre illustri le caratteristiche dei dispositivi di conversione A/D e D/A che intende utilizzare.

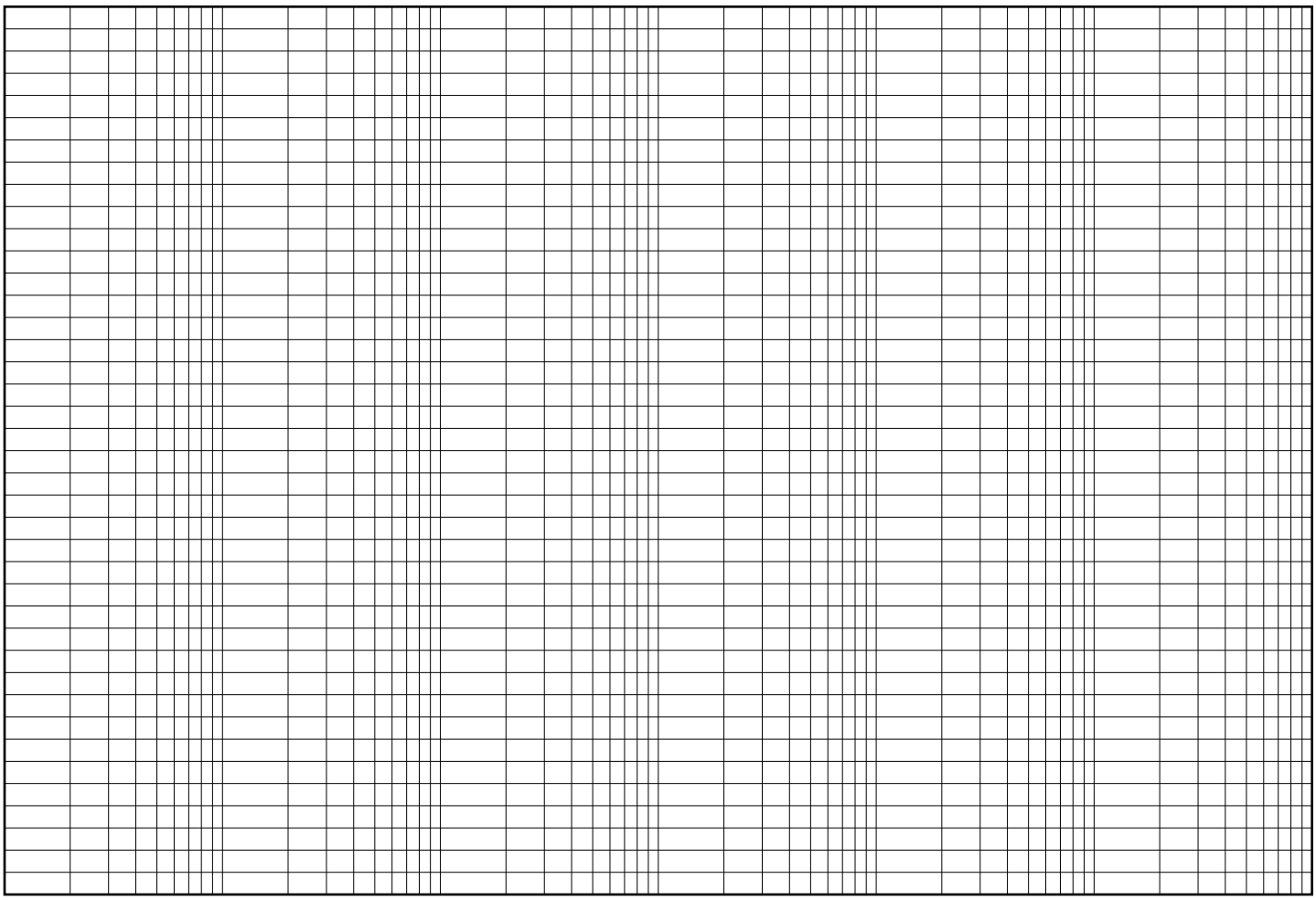
Per semplicità di risoluzione si consiglia di preferire un progetto per sintesi diretta oppure per retroazione dagli stati con osservatore al progetto in frequenza.

Nota: l'eventuale tracciamento di diagrammi di Bode e/o di Nichols sia fatto sugli appositi fogli da richiedersi alla Commissione.

Carta semilogaritmica a 6 decadi

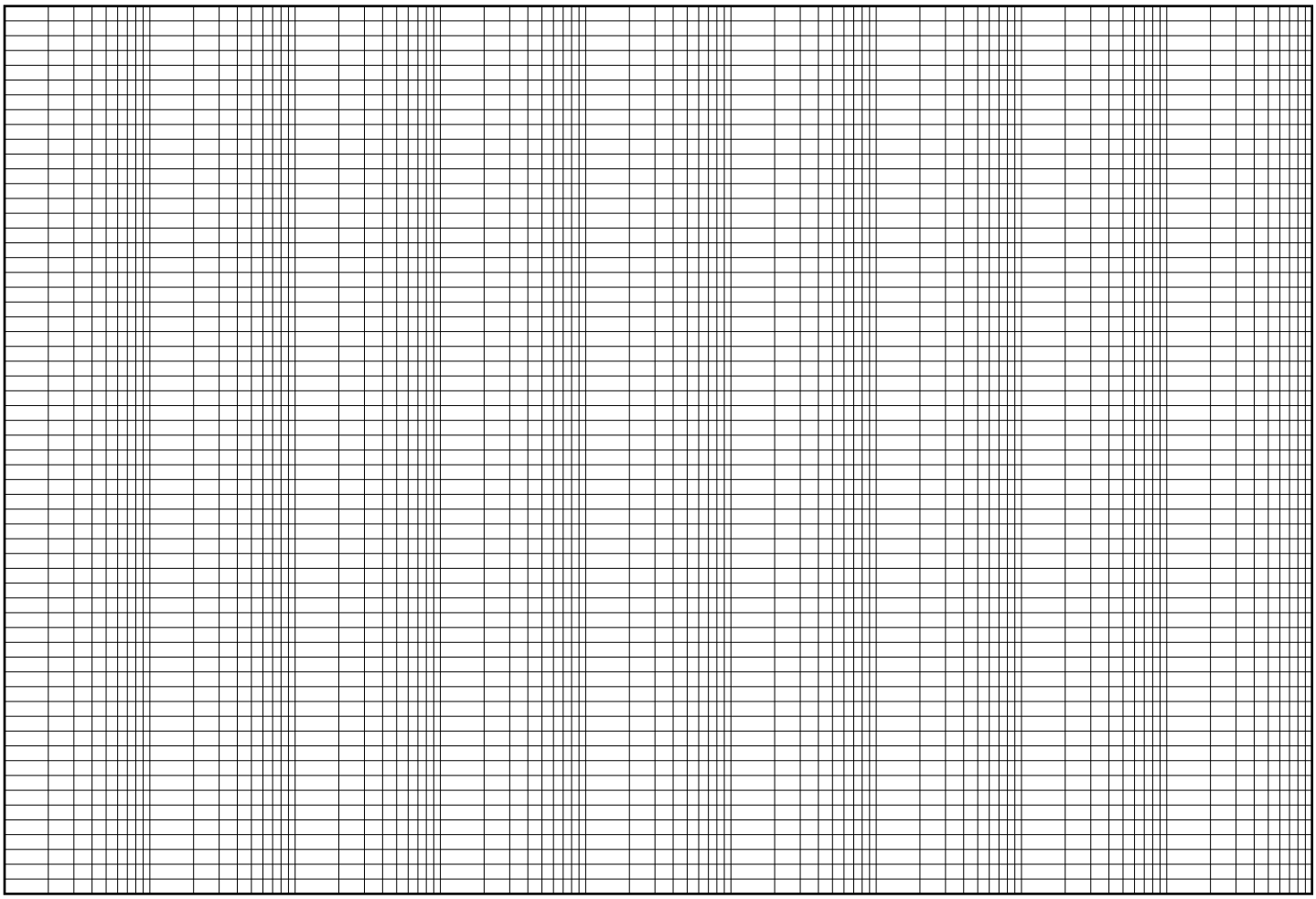


Pulsazione ω

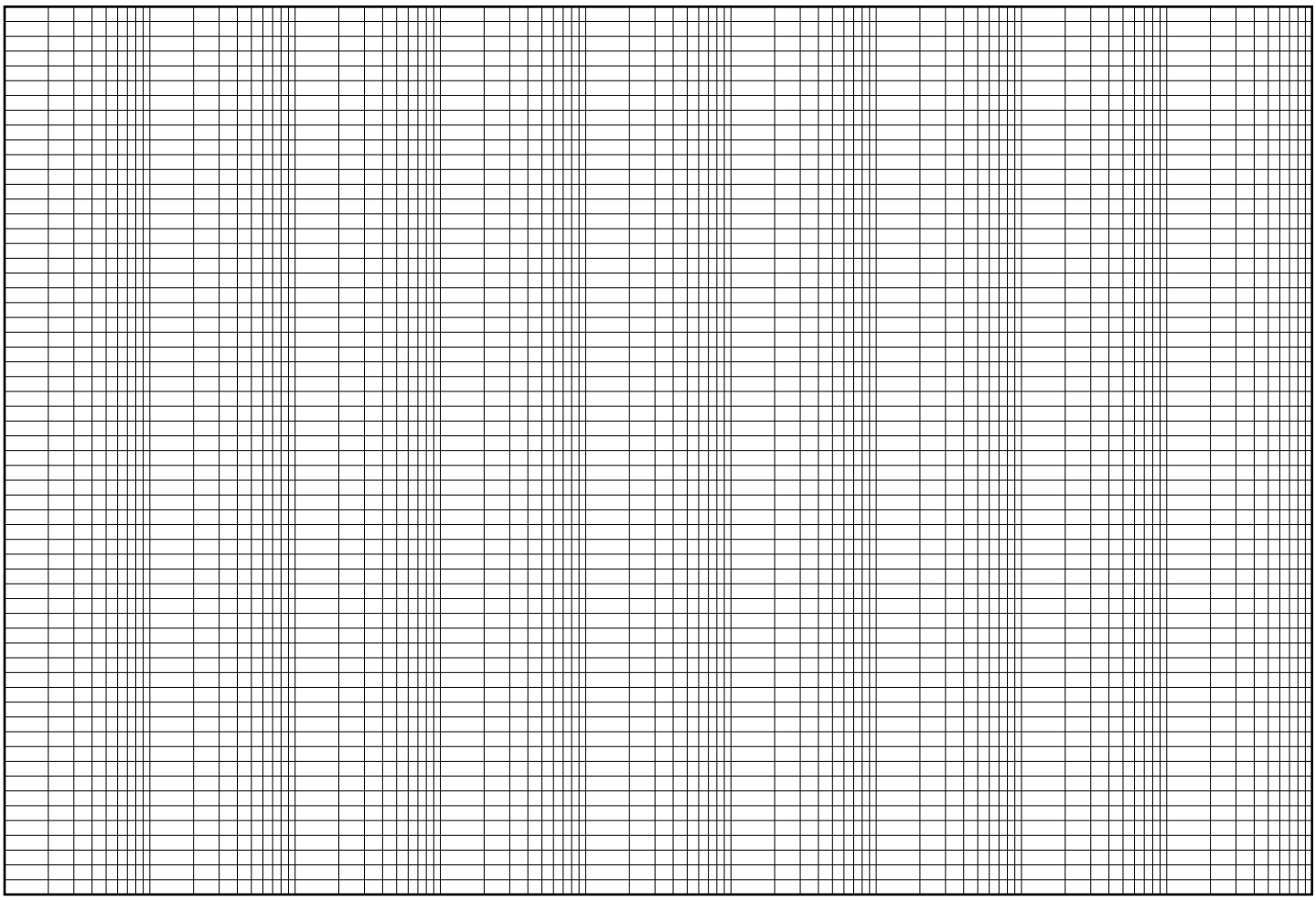


Pulsazione ω

Carta semilogaritmica a 9 decadi



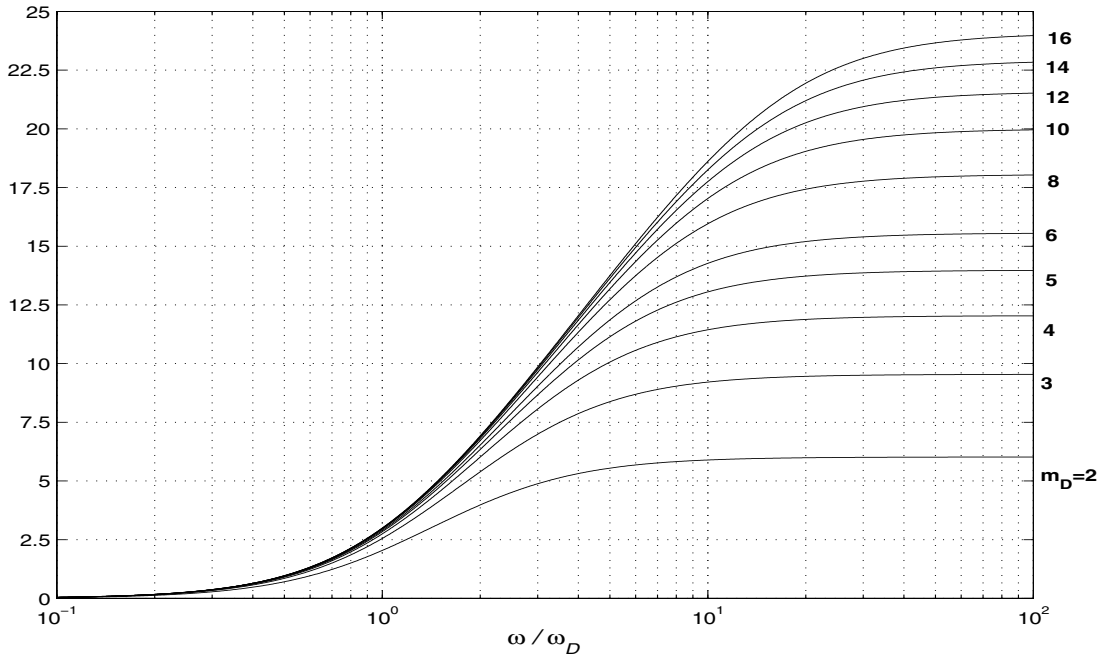
Pulsazione ω

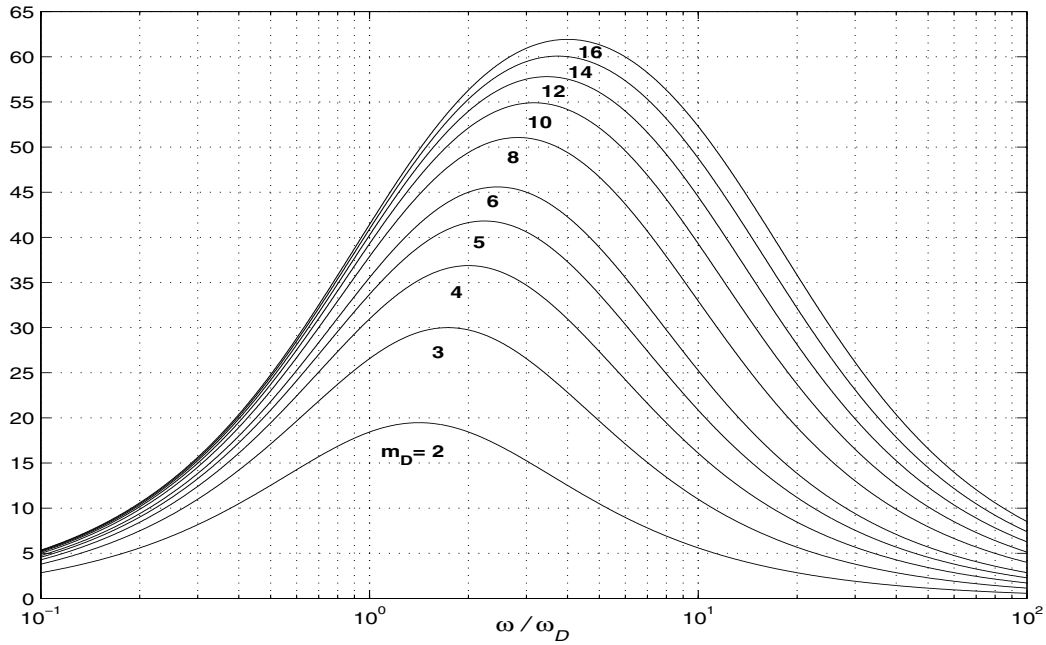


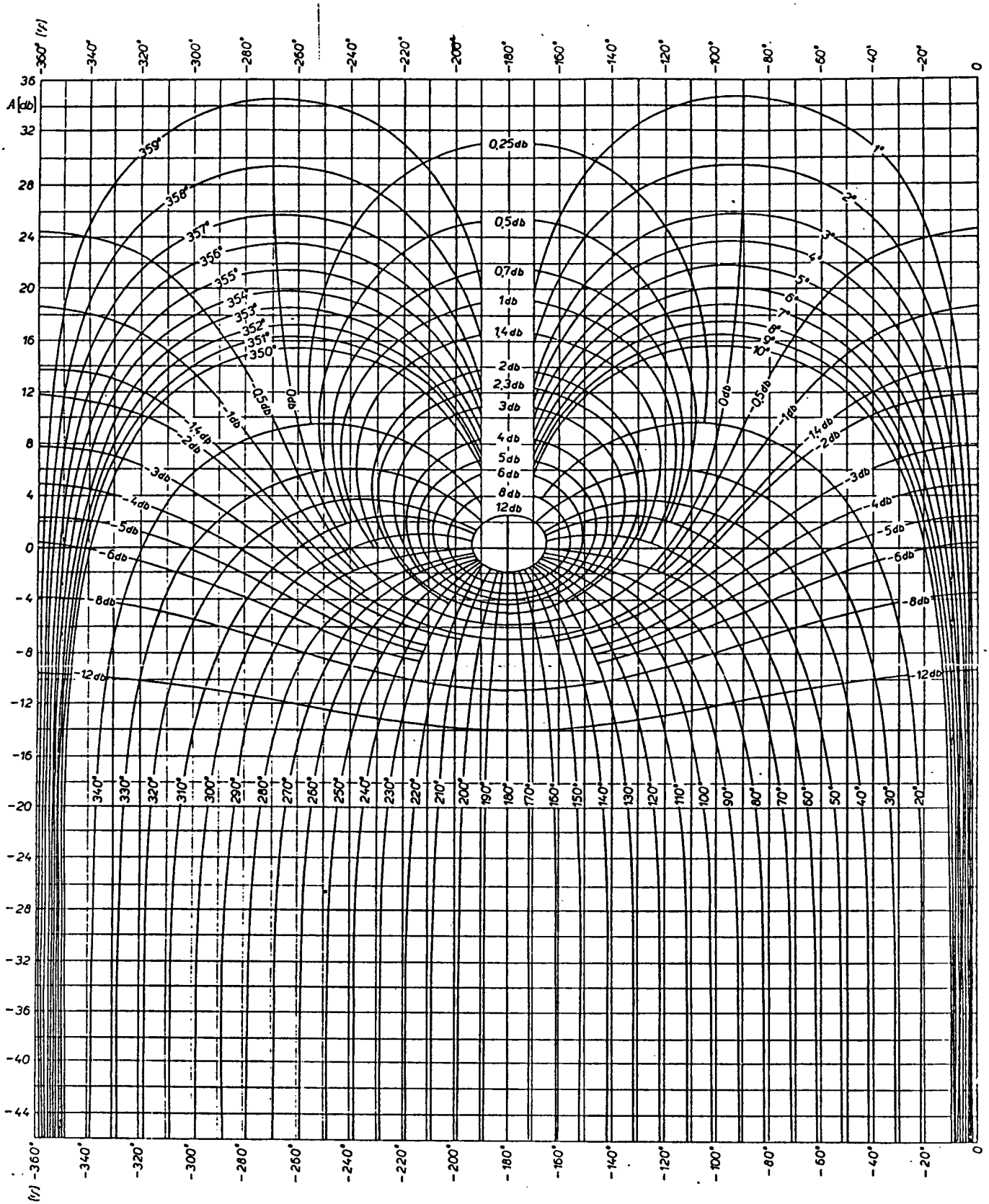
Pulsazione ω

Funzione Anticipatrice

$$C_D(s) = \frac{1 + \dfrac{s}{\omega_D}}{1 + \dfrac{s}{m_D \omega_D}}, \; m_D > 1$$







Carta di Nichols

Tema n. 3

Si deve progettare un sistema radio capace di trasmettere su un canale di trasmissione di ampiezza totale pari a 10 MHz, attorno alla frequenza di trasmissione di 18 GHz. La bit-rate minima da garantire è pari a 20 Mbps su una distanza pari a 5 km. Si supponga di utilizzare una modulazione a singola portante con filtri di trasmissione e di ricezione del tipo a coseno rialzato con coefficiente di roll-off pari a 0.2.

1. Si scelgano valori realistici per le seguenti grandezze e parametri:
    a. Potenza di trasmissione
    b. Tipo e guadagni di antenna in trasmissione ed in ricezione
    c. Cifra di rumore del ricevitore

   Come canale di trasmissione semplificato si consideri in prima battuta un collegamento in piena vista e si considerino poi perdite aggiuntive dovute a pioggia, attenuazioni atmosferiche, margine di implementazione dell'ordine di 15 dB.

2. Si progetti la modulazione da utilizzare (se necessario, si facciano ipotesi realistiche di progetto su ogni altra grandezza coinvolta).
3. Si calcoli il rapporto segnale-disturbo in ricezione e si calcoli in modo approssimato il valore di Bit Error Rate conseguito in ricezione.
4. Si discuta il possibile vantaggio di una modulazione multiportante OFDM nel caso di trasmissione su canale con multipath. Si identifichino i punti critici di progetto in questo caso.

   Il sistema viene utilizzato per distribuire filmati video.
5. Si facciano ipotesi realistiche sulle velocità dei filmati, motivandole in base alla qualità del video.
6. Si spieghi quali sistemi di multiplazione possono essere utilizzati per trasmettere più video in contemporanea mediante questo sistema radio.
7. Si discuta almeno uno dei due punti seguenti:
    a. Procedure di posizionamento meccanico e puntamento delle antenne.
    b. Normative da osservare in relazione all'esposizione da campi elettromagnetici in base alle normative vigenti.

I candidati tengano presente che, oltre alla correttezza dei risultati, verranno valutati l'*ordine e la chiarezza* dell'elaborato, indicatori essenziali della maturità professionale acquisita.

Tema n. 4

Un edificio di recente costruzione, costituito da due piani e seminterrato, ospita una scuola superiore con circa 1500 studenti. Negli uffici di segreteria e presidenza, situati al piano terra, ci sono 15 postazioni di lavoro fisse connesse da un'infrastruttura di rete Ethernet con apparati a 100 Mb/s. Questa rete, di seguito denominata "rete amministrativa", è collegata ad Internet attraverso una linea ADSL a 7 Mb/s.

I computer presenti nei 10 laboratori didattici e le altre postazioni fisse a disposizione dei docenti sono anch'essi collegati tramite una seconda rete Ethernet, di seguito denominata "rete didattica", con apparati a 100 Mb/s. Essa è totalmente separata da quella amministrativa e si connette alla rete Internet mediante una seconda linea ADSL a 24 Mb/s. L'attuale separazione fisica delle due reti garantisce che le informazioni trattate all'interno della rete amministrativa non siano accessibili dalla rete didattica.

La scuola ha però esigenze crescenti sui servizi di rete, sia per quanto riguarda l'attività amministrativa, sempre più viene svolta su portali esterni ministeriali e privati, sia per quanto riguarda la didattica innovativa e multimediale. Per questo motivo la scuola intende aggiornare la sua infrastruttura al fine di conseguire i seguenti obiettivi:

a) per l'accesso ordinario ad Internet, sostituire le due linee ADSL con un'unica linea più performante, alla quale connettere sia la rete didattica, sia quella amministrativa, pur continuando a mantenere separato il traffico delle due reti e pur continuando a mantenere una linea ADSL, delle due preesistenti, come linea di riserva in caso di malfunzionamenti sulla nuova.
b) aumentare la banda disponibile per i computer presenti nei laboratori didattici e dei docenti;
c) offrire una piattaforma interna per la didattica multimediale e per servizi in streaming, accessibile sia dalla rete locale interna alla scuola, sia tramite Internet;
d) garantire la sicurezza della rete interna da possibili minacce, sia interne che esterne, e la privacy degli utilizzatori;

Il candidato, come responsabile (ex art. 46 del DPR 328/01) di pianificazione, progettazione, sviluppo, direzione lavori, stima, collaudo e gestione di impianti e sistemi elettronici, di automazione e di generazione, trasmissione ed elaborazione delle informazioni, formulando le opportune ipotesi aggiuntive, sviluppi i seguenti punti:

1. rappresenti graficamente uno schema logico dell'infrastruttura di rete esistente;
2. proponga un progetto per l'evoluzione di tale infrastruttura, che soddisfi le esigenze sopra esplicitate, indicando le risorse hardware e software necessarie; approfondendo in particolare le caratteristiche della nuova connessione Internet, i meccanismi per mantenere la separazione del traffico tra le due reti interne, la migrazione degli apparati, gli strumenti di sicurezza, la gestione della linea ADSL di riserva;
3. proponga i principali servizi da implementare, esemplificando le relative configurazioni per almeno uno di essi;
4. specifichi le misure necessarie a prevenire le possibili interruzioni dei vari servizi offerti;
5. immagini di voler gestire sul server web un sistema di news interne alla scuola e ne progetti lo schema concettuale e logico della base di dati.

Inoltre, poiché la scuola intende sviluppare, almeno per le classi superiori, una didattica basata sull'utilizzo in classe dei dispositivi mobili degli studenti (smartphone, tablet, PC portatili) con accesso ad internet, il candidato tratti la tematica BYOD (Bring Your Own Device) applicata al caso, in particolare evidenziando:

- l'hardware ed i servizi necessari per la realizzazione di tale didattica;
- le modalità per filtrare e modulare gli accessi a docenti, studenti ed eventuali altri utilizzatori;
- le problematiche prevedibili e le possibili soluzioni.

Tema n. 5

Il candidato progetti un sistema di acquisizione e memorizzazione di alcuni parametri ambientali, fra cui le temperature interna ed esterna di un ambiente, la sua umidità relativa e la pressione atmosferica, avente preferibilmente le seguenti caratteristiche:

1) Temperature interna ed esterna:
    a. Intervallo di misura: -20°C ... +60°C
    b. Accuratezza: +/- 0.5°C
    c. Unità di misura della memorizzazione: 1K
    d. Risoluzione della memorizzazione: 1/8 K
    e. Frequenza di acquisizione: 1 campione/s per ciascun sensore
2) Pressione assoluta:
    a. Intervallo di misura: 90kPa … 110kPa
    b. Accuratezza: +/- 2kPa
    c. Unità di misura della memorizzazione: 1kPa
    d. Risoluzione della memorizzazione: 1/16 kPa
    e. Frequenza di acquisizione: 1 campione/min
3) Umidità relativa:
    a. Intervallo di misura: 10% … 90%
    b. Accuratezza: +/- 2%
    c. Unità di misura della memorizzazione: 1%
    d. Risoluzione della memorizzazione: 1/4 %
    e. Frequenza di acquisizione: 4 campioni/min
4) Capacità di memoria:
    a. Minimo 1 anno di campionamento continuo di tutti i parametri menzionati
5) Sorgente di alimentazione:
    a. Il sistema dovrà funzionare con due, tre o quattro batterie tipo AAA
    b. Il sistema dovrà essere progettato per massimizzare la durata delle batterie, che non dovrà essere inferiore a 1 anno.

Il candidato dovrà, nell'ordine:

1) Ipotizzare e descrivere operativamente alcune funzionalità del sistema, che contemplino almeno la possibilità di avviare e terminare l'acquisizione dei dati, di scaricare i dati su un PC (in qualunque modalità a scelta del candidato), di accendere e spegnere il sistema quando non viene utilizzato, di cambiare le batterie quando viene segnalato un basso livello di carica.
2) Selezionare i tre trasduttori o sensori di temperatura, pressione, umidità, eventualmente selezionandoli fra quelli proposti o, se si preferisce, qualunque altro modello commercialmente disponibile (in quest'ultimo caso, citando chiaramente modello e costruttore).
3) Sviluppare il progetto architetturale del sistema e predisporre uno schema a blocchi completo del sistema, ove siano inclusi almeno tutti gli elementi HW e SW necessari al funzionamento del sistema secondo le modalità operative definite al punto precedente.
4) Si scelga un microcontrollore adatto al sistema, eventualmente scegliendo il modello MSP430F5438 della Texas Instruments di cui viene dato stralcio del datasheet.
5) Sviluppare lo schema elettrico di:
    a. Sensore di temperatura
    b. Sensore di pressione
    c. Sensore di umidità

Tali da poter essere connessi direttamente all'alimentazione interna e agli ingressi analogici e/o digitali del microcontrollore.
Almeno uno dei tre dovrà avere un'uscita analogica.
I circuiti dovranno essere tali da poter soddisfare globalmente il requisito di durata delle batterie.

6) Si imposti il diagramma di flusso del SW di acquisizione.
7) Si sviluppi, in qualsiasi linguaggio compilabile per microcontrollore la routine di inizializzazione dell'ADC del microcontrollore selezionato.
8) Si stimi la durata delle batterie, considerando un uso continuativo ed il funzionamento definito dal diagramma di flusso sviluppato in precedenza

Allegati al testo d'esame:

1) Stralcio datasheet microcontrollore MSP430F5438
2) Stralcio user guide dell'ADC12 del MSP430F5438
3) Stralcio datasheet sensore temperatura LM76
4) Stralcio datasheet sensore temperatura LM35
5) Stralcio datasheet sensore temperatura BD1020
6) Stralcio datasheet sensore pressione KP235
7) Stralcio datasheet sensore umidità e temperatura ChipCap
8) Stralcio datasheet OP-AMP OPA378
9) Stralcio datasheet OP-AMP TSB611
10) Stralcio datasheet batteria primaria 1212

MSP430F543xA, MSP430F541xA Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low Supply Voltage Range:
  3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
  - Active Mode (AM):
    All System Clocks Active
    230 µA/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
    110 µA/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3):
    Real-Time Clock (RTC) With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
    1.7 µA at 2.2 V, 2.1 µA at 3.0 V (Typical)
    Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
    1.2 µA at 3.0 V (Typical)
  - Off Mode (LPM4):
    Full RAM Retention, Supply Supervisor Operational, Fast Wakeup:
    1.2 µA at 3.0 V (Typical)
  - Shutdown Mode (LPM4.5):
    0.1 µA at 3.0 V (Typical)
- Wake up From Standby Mode in 3.5 µs (Typical)
- 16-Bit RISC Architecture
  - Extended Memory
  - Up to 25-MHz System Clock
- Flexible Power-Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Crystals
  - High-Frequency Crystals up to 32 MHz
- 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer_B With Seven Capture/Compare Shadow Registers
- Up to Four Universal Serial Communication Interfaces
  - USCI_A0, USCI_A1, USCI_A2, and USCI_A3 Each Support:
    - Enhanced UART Supports Automatic Baud-Rate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0, USCI_B1, USCI_B2, and USCI_B3 Each Support:
    - I^2C
    - Synchronous SPI
- 12-Bit Analog-to-Digital Converter (ADC)
  - Internal Reference
  - Sample-and-Hold
  - Autoscan Feature
  - 14 External Channels, 2 Internal Channels
- Hardware Multiplier Supports 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three-Channel Internal DMA
- Basic Timer With RTC Feature
- Section 3 Summarizes the Available Family Members
- For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208)

1.2 Applications

- Analog and Digital Sensor Systems
- Digital Motor Controls
- Remote Controls
- Thermostats
- Digital Timers
- Hand-Held Meters

1.3 Description

The TI MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5 µs (typical).

The MSP430F543xA and MSP430F541xA series are microcontroller configurations with three 16-bit timers, a high-performance 12-bit ADC, up to four universal serial communication interfaces (USCIs), a hardware multiplier, DMA, an RTC module with alarm capabilities, and up to 87 I/O pins.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, and hand-held meters.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430F5438AZQW	MicroStar Junior™ BGA (113)	7 mm × 7 mm
MSP430F5438APZ	LQFP (100)	14 mm × 14 mm
MSP430F5437APN	LQFP (80)	12 mm × 12 mm

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.

1.4 Functional Block Diagrams

Figure 1-1 and Figure 1-2 show the functional block diagrams.

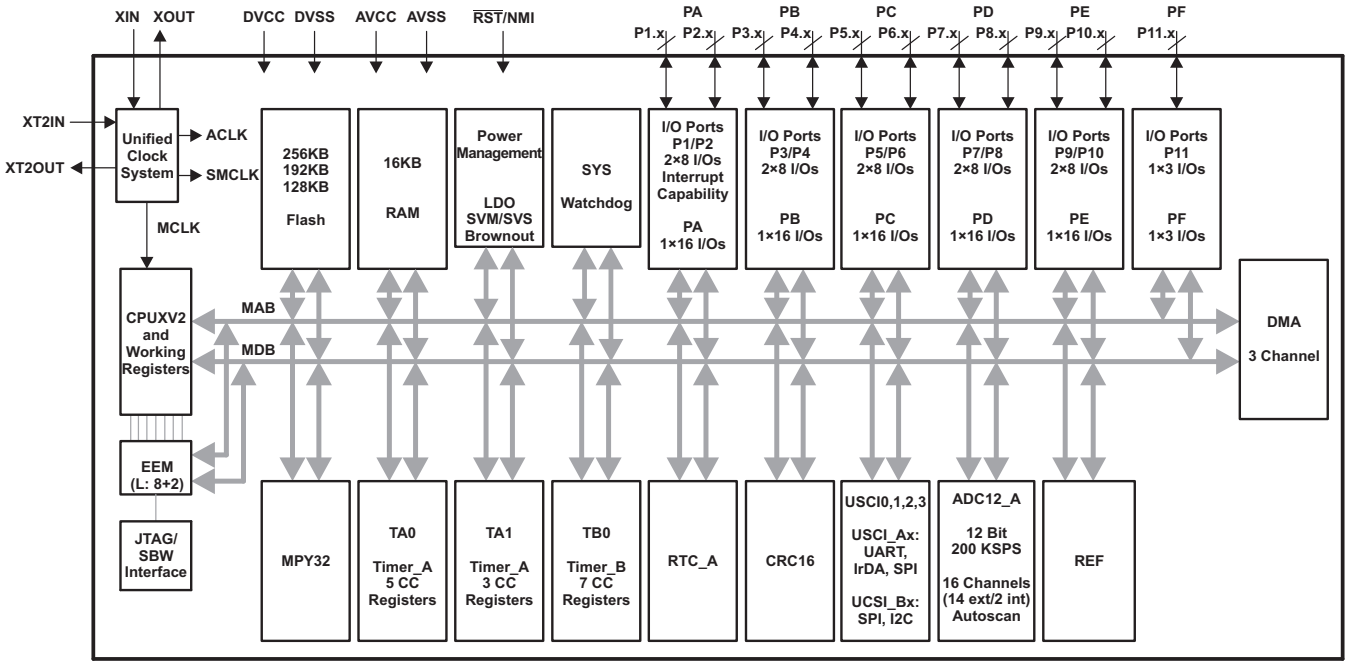


Figure 1-1. Functional Block Diagram – MSP430F5438AIPZ, MSP430F5436AIPZ, MSP430F5419AIPZ, MSP430F5438AIZQW, MSP430F5436AIZQW, MSP430F5419AIZQW

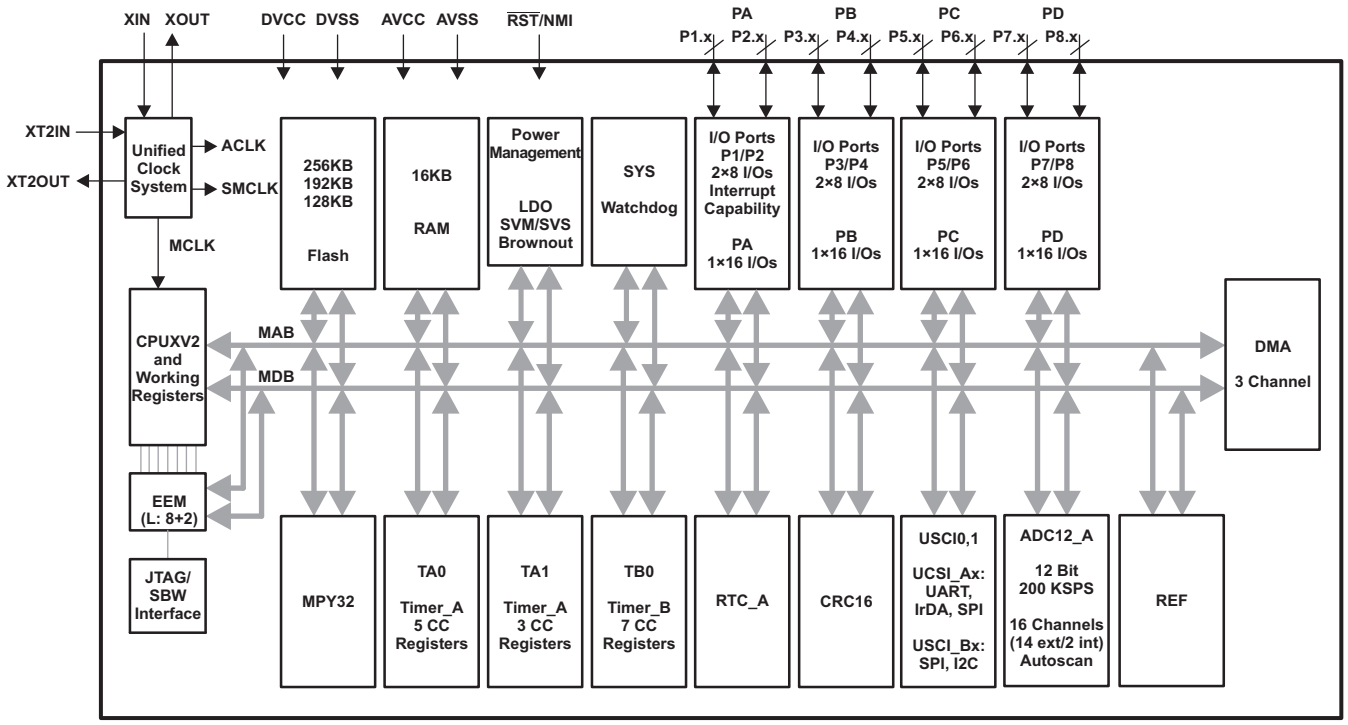


Figure 1-2. Functional Block Diagram – MSP430F5437AIPN, MSP430F5435AIPN, MSP430F5418AIPN

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Family Members(1)(2)

DEVICE	FLASH (KB)	SRAM (KB)	Timer_A(3)	Timer_B(4)	USCI		ADC12_A (Ch)	I/O	PACKAGE
					CHANNEL A: UART, IrDA, SPI	CHANNEL B: SPI, I^2C			
MSP430F5438A	256	16	5, 3	7	4	4	14 ext, 2 int	87	100 PZ, 113 ZQW
MSP430F5437A	256	16	5, 3	7	2	2	14 ext, 2 int	67	80 PN
MSP430F5436A	192	16	5, 3	7	4	4	14 ext, 2 int	87	100 PZ, 113 ZQW
MSP430F5435A	192	16	5, 3	7	2	2	14 ext, 2 int	67	80 PN
MSP430F5419A	128	16	5, 3	7	4	4	14 ext, 2 int	87	100 PZ, 113 ZQW
MSP430F5418A	128	16	5, 3	7	2	2	14 ext, 2 int	67	80 PN

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators.

5 Specifications

5.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
Voltage applied to any pin (excluding VCORE)[2]	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} [3]	–55	105	°C
Maximum junction temperature, T_J		95	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

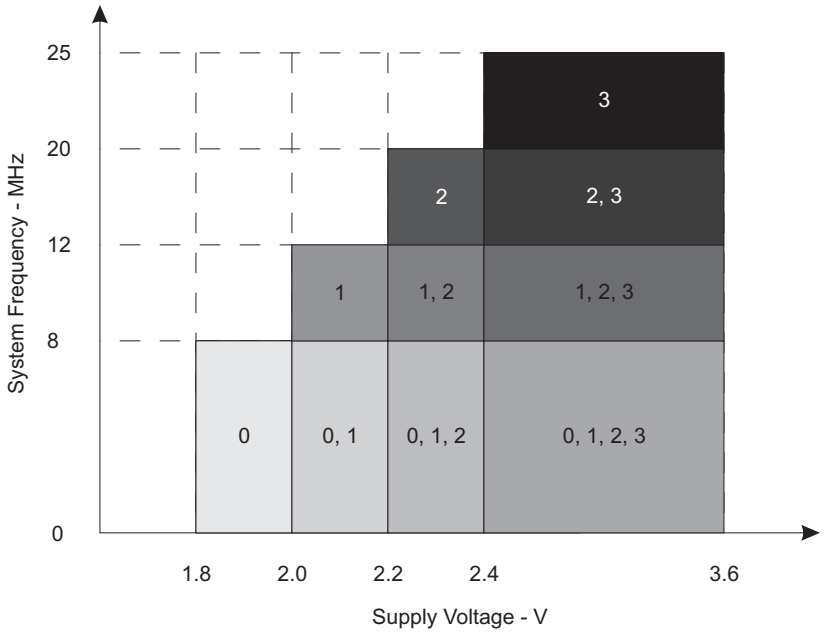
(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (AV_{CC} = $DV_{CC1/2/3/4}$ = DV_{CC})[1][2]		1.8		3.6	V
V_{SS}	Supply voltage (AV_{SS} = $DV_{SS1/2/3/4}$ = DV_{SS})			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{VCORE}	Recommended capacitor at VCORE[3]			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[4] [5] (see Figure 5-1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V	0		8	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0		12	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		20	
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		25	

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Section 5.23 threshold parameters for the exact values and further details.
(3) A capacitor tolerance of ±20% or better is required.
(4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Frequency vs Supply Voltage

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$	Flash	3.0 V	0	0.29	0.33	1.84	2.08							mA
			1	0.32		2.08		3.10						
			2	0.33		2.24		3.50		6.37				
			3	0.35		2.36		3.70		6.75		8.90	9.60	
$I_{AM, RAM}$	RAM	3.0 V	0	0.17	0.19	0.88	0.99							mA
			1	0.18		1.00		1.47						
			2	0.19		1.13		1.68		2.82				
			3	0.20		1.20		1.78		3.00		4.50	4.90	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1][2]

PARAMETER		V_{CC}	PMMCOREVx	–40°C		25°C		60°C		85°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0[3][4]	2.2 V	0	69	93	69	93	69	93	69	93	µA
		3.0 V	3	73	100	73	100	73	100	73	100	
I_{LPM2}	Low-power mode 2[5][4]	2.2 V	0	11	15.5	11	15.5	11	15.5	11	15.5	µA
		3.0 V	3	11.7	17.5	11.7	17.5	11.7	17.5	11.7	17.5	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode[6][4]	2.2 V	0	1.4		1.7		2.6		6.6		µA
			1	1.5		1.8		2.9		9.9		
			2	1.5		2.0		3.3		10.1		
		3.0 V	0	1.8		2.1	2.4	2.8		7.1	13.6	
			1	1.8		2.3		3.1		10.5		
			2	1.9		2.4		3.5		10.6		
			3	2.0		2.3	2.6	3.9		11.8	14.8	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode[7][4]	3.0 V	0	1.0		1.2	1.42	2.0		5.8	12.9	µA
			1	1.0		1.3		2.3		6.0		
			2	1.1		1.4		2.8		6.2		
			3	1.2		1.4	1.62	3.0		6.2	13.9	
I_{LPM4}	Low-power mode 4[8][4]	3.0 V	0	1.1		1.2	1.35	1.9		5.7	12.9	µA
			1	1.2		1.2		2.2		5.9		
			2	1.3		1.3		2.6		6.1		
			3	1.3		1.3	1.52	2.9		6.2	13.9	
$I_{LPM4.5}$	Low-power mode 4.5[9]	3.0 V		0.10		0.10	0.13	0.20		0.50	1.14	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
(4) Current for brownout, high side supervisor (SVS_H) normal mode included. Low-side supervisor and monitors disabled (SVS_L, SVM_L). High-side monitor disabled (SVM_H). RAM retention enabled.
(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz, DCO setting = 1 MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
(9) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

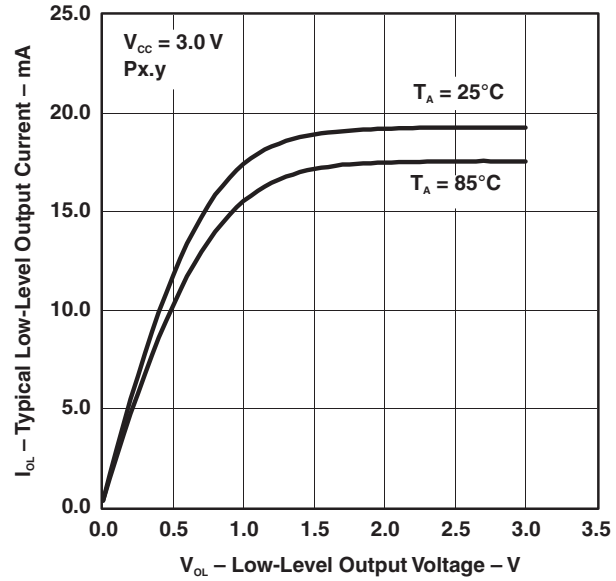


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

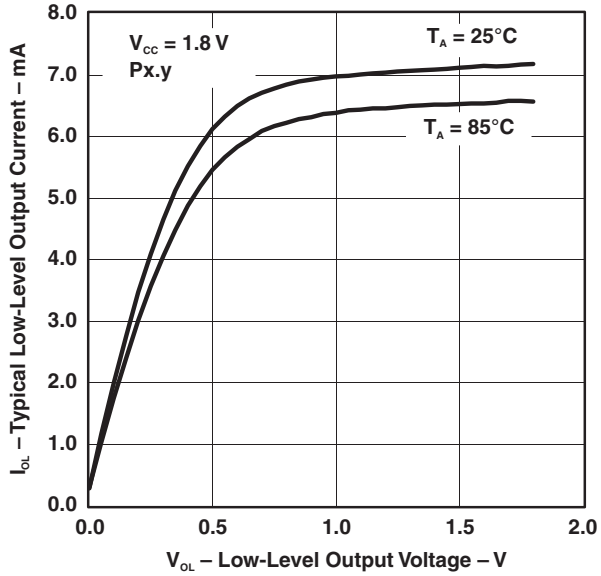


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

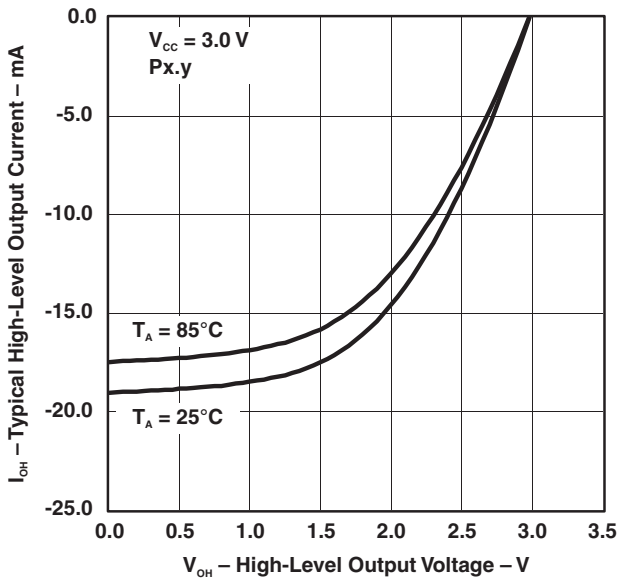


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

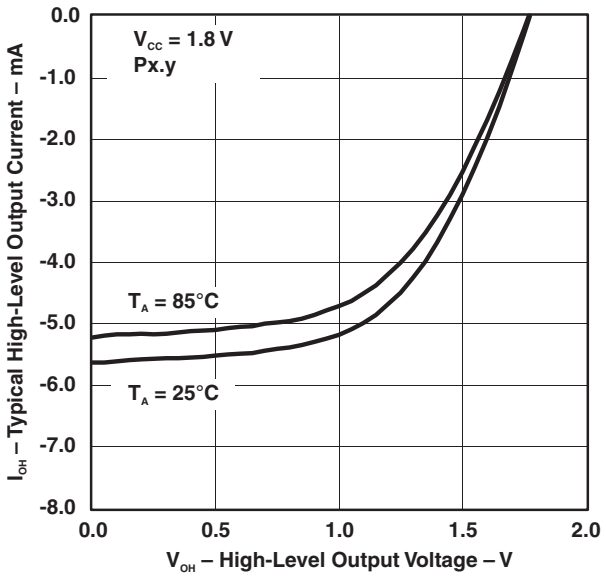


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.36 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range[2]	All ADC12 analog input pins Ax		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AVCC terminal[3]	$f_{ADC12CLK}$ = 5.0 MHz[4]	2.2 V		125	155	µA
			3 V		150	220	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R_I	Input MUX ON-resistance	$0 V \le V_{Ax} \le AVCC$		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See Section 5.41 and Section 5.42.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.
(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

5.37 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC conversion clock	For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference.[1]	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference.[2]		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference.[3]		0.45	2.4	2.7	
$f_{ADC12OSC}$	Internal ADC12 oscillator[4]	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			[5]		
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 20 pF, $\tau = [R_S + R_I] \times C_I$ [6]	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5.0 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(5) $13 \times ADC12DIV \times 1/f_{ADC12CLK}$
(6) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

5.38 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(1)	1.4 V ≤ dVREF ≤ 1.6 V(2)	2.2 V, 3 V			±2.0	LSB
		1.6 V < dVREF(2)				±1.7	
E_D	Differential linearity error(1)	(2)	2.2 V, 3 V			±1.0	LSB
E_O	Offset error(3)	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±1.0	±2.0	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±1.0	±2.0	
E_G	Gain error(3)	(2)	2.2 V, 3 V		±1.0	±2.0	LSB
E_T	Total unadjusted error	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±1.4	±3.5	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±1.4	±3.5	

(1) Parameters are derived using the histogram method.
(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = $V_{R+} – V_{R–}$, V_{R+} < AVCC, $V_{R–}$ > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).
(3) Parameters are derived using a best fit curve.

5.39 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V			±1.7	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±2.5	
E_D	Differential linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V	–1.0		+1.5	LSB
		ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 2.7 MHz		–1.0		+1.0	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz		–1.0		+2.5	
E_O	Offset error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2.0	±4.0	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±2.0	±4.0	
E_G	Gain error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1.0	±2.5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1.5%(4)	VREF
E_T	Total unadjusted error	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2	±5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1.5%(4)	VREF

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = $V_{R+} – V_{R–}$.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

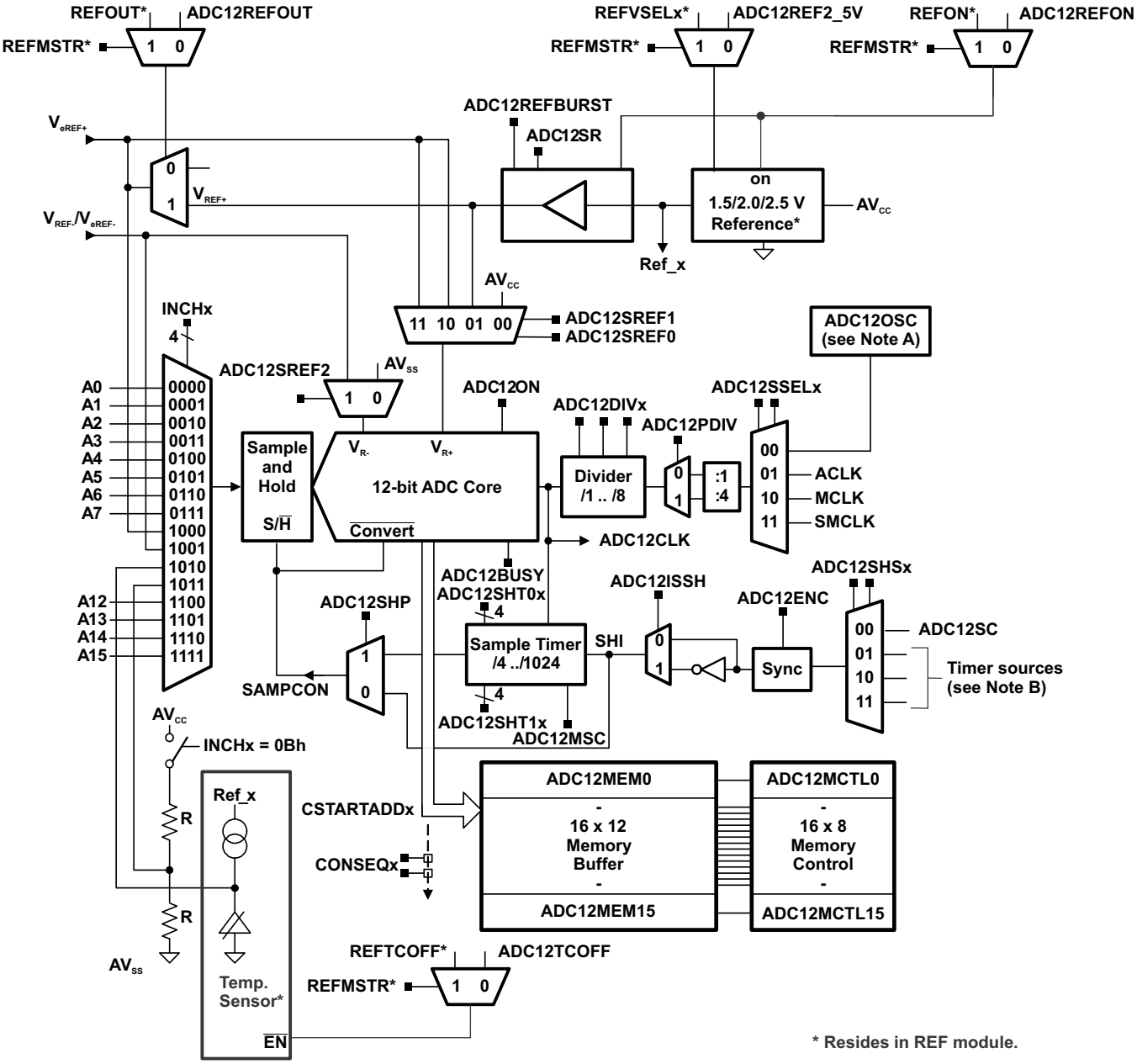
28.1 ADC12_A Introduction

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator (MSP430F54xx (non-A only) – in other devices, separate REF module), and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

ADC12_A features include:

- Greater than 200-ksps maximum conversion rate
- Monotonic 12-bit converter with no missing codes
- Sample-and-hold with programmable sampling periods controlled by software or timers
- Conversion initiation by software or timers
- Software-selectable on-chip reference voltage generation (MSP430F54xx (non-A only): 1.5 V or 2.5 V, all other devices: 1.5 V, 2.0 V, or 2.5 V)
- Software-selectable internal or external reference
- Up to 12 individually configurable external input channels
- Conversion channels for internal temperature sensor, AV_{CC}, and external references
- Independent channel-selectable reference sources for both positive and negative references
- Selectable conversion clock source
- Single-channel, repeat-single-channel, sequence (autoscan), and repeat-sequence (repeated autoscan) conversion modes
- ADC core and reference voltage can be powered down separately
- Interrupt vector register for fast decoding of 18 ADC interrupts
- 16 conversion-result storage registers

The block diagram of ADC12_A is shown in Figure 28-1. In MSP430F54xx (non-A only), the reference generator is located in the ADC12_A module itself. In other devices, the reference generator is located in the reference module, REF. See the REF module chapter and the device-specific data sheet for further details. Figure 28-1 shows the block diagram for devices that have the REF module available. Figure 28-2 shows the block diagram for the MSP430F54xx (non-A only) which does not incorporate the REF module.



A ADC12OSC refers to the MODCLK from the UCS. See the UCS chapter for more information.

B See the device-specific data sheet for timer sources available.

Figure 28-1. ADC12_A Block Diagram (Devices With REF Module)

28.2 ADC12_A Operation

The ADC12_A module is configured with user software. The setup and operation of the ADC12_A is discussed in the following sections.

28.2.1 12-Bit ADC Core

The ADC core converts an analog input to its 12-bit digital representation and stores the result in conversion memory. The core uses two programmable and selectable voltage levels (V_{R+} and V_{R-}) to define the upper and lower limits of the conversion. The digital output (N_{ADC}) is full scale (0FFFh) when the input signal is equal to or higher than V_{R+}. The digital output (N_{ADC}) is zero when the input signal is equal to or lower than V_{R-}. The input channel and the reference voltage levels (V_{R+} and V_{R-}) are defined in the conversion-control memory. The conversion formula for the ADC result N_{ADC} is:

$$N_{ADC} = 4095 \times \frac{Vin - V_{R-}}{V_{R+} - V_{R-}}$$

The ADC12_A core is configured by two control registers, ADC12CTL0 and ADC12CTL1. The core is enabled with the ADC12ON bit. The ADC12_A can be turned off when it is not in use to save power. With few exceptions, the ADC12_A control bits can be modified only when ADC12ENC = 0. ADC12ENC must be set to 1 before any conversion can take place.

28.2.1.1 Conversion Clock Selection

The ADC12CLK is used both as the conversion clock and to generate the sampling period when the pulse sampling mode is selected. The ADC12_A source clock is selected using the predivider controlled by the ADC12PDIV bit and the divider using the ADC12SSELx bits. The input clock can be divided from 1 to 32 using both the ADC12DIVx bits and the ADC12PDIV bit. Possible ADC12CLK sources are SMCLK, MCLK, ACLK, and the ADC12OSC.

The ADC12OSC in the block diagram (see Figure 28-1) refers to the MODCLK 5-MHz oscillator from the UCS (see the UCS module for more information) which can vary with individual devices, supply voltage, and temperature. See the device-specific data sheet for the ADC12OSC specification.

The user must ensure that the clock chosen for ADC12CLK remains active until the end of a conversion. If the clock is removed during a conversion, the operation does not complete and the results are invalid.

28.2.2 ADC12_A Inputs and Multiplexer

The 12 external and 4 internal analog signals are selected as the channel for conversion by the analog input multiplexer. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching (see Figure 28-3). The input multiplexer is also a T-switch to minimize the coupling between channels. Channels that are not selected are isolated from the ADC, and the intermediate node is connected to analog ground (AV_{SS}) so that the stray capacitance is grounded to eliminate crosstalk.

The ADC12_A uses the charge redistribution method. When the inputs are internally switched, the switching action may cause transients on the input signal. These transients decay and settle before causing errant conversion.

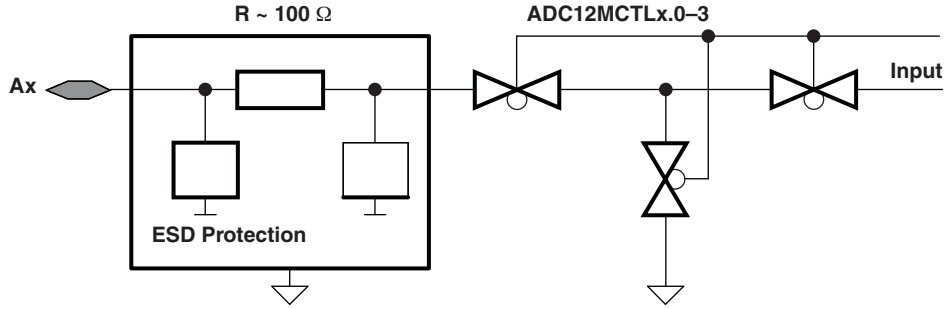


Figure 28-3. Analog Multiplexer

The internal reference buffer also has selectable speed versus power settings. When the maximum conversion rate is below 50 ksps, setting ADC12SR = 1 reduces the current consumption of the buffer by approximately 50%.

28.2.4 Auto Power Down

The ADC12_A is designed for low-power applications. When the ADC12_A is not actively converting, the core is automatically disabled, and it is automatically reenabled when needed. The MODOSC is also automatically enabled when needed and disabled when not needed.

28.2.5 Sample and Conversion Timing

An analog-to-digital conversion is initiated with a rising edge of the sample input signal SHI. The source for SHI is selected with the SHSx bits and includes the following:

- ADC12SC bit
- Up to three timer outputs (see the device-specific data sheet for available timer sources)

The ADC12_A supports 8-bit, 10-bit, and 12-bit resolution modes selectable by the ADC12RES bits. The analog-to-digital conversion requires 9, 11, and 13 ADC12CLK cycles, respectively. The polarity of the SHI signal source can be inverted with the ADC12ISSH bit. The SAMPCON signal controls the sample period and start of conversion. When SAMPCON is high, sampling is active. The high-to-low SAMPCON transition starts the analog-to-digital conversion. Two different sample-timing methods are defined by control bit ADC12SHP, extended sample mode and pulse mode. See the device-specific data sheet for available timers for SHI sources.

28.2.5.1 Extended Sample Mode

The extended sample mode is selected when ADC12SHP = 0. The SHI signal directly controls SAMPCON and defines the length of the sample period t_{sample}. When SAMPCON is high, sampling is active. The high-to-low SAMPCON transition starts the conversion after synchronization with ADC12CLK (see Figure 28-4).

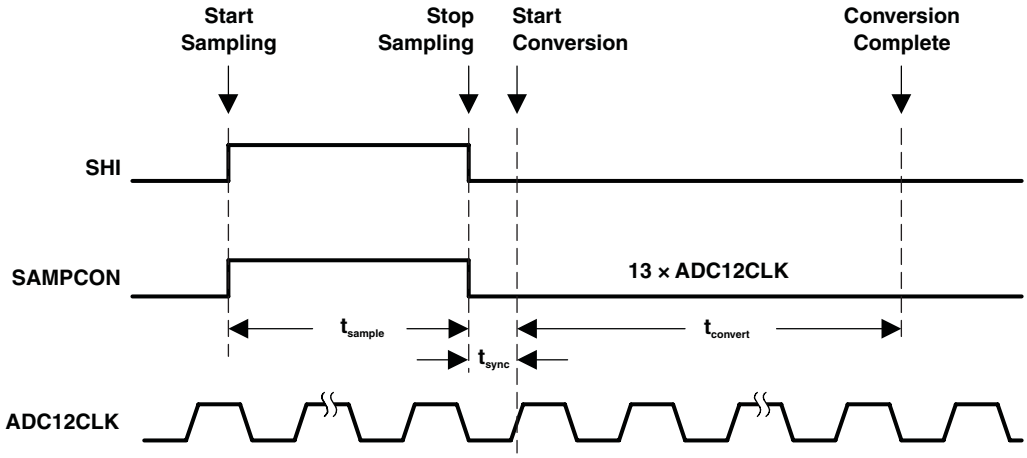


Figure 28-4. Extended Sample Mode

28.2.5.2 Pulse Sample Mode

Set ADC12SHP = 1 to select the pulse sample mode. The SHI signal is used to trigger the sampling timer. The ADC12SHT0x and ADC12SHT1x bits in ADC12CTL0 control the interval of the sampling timer that defines the SAMPCON sample period t_{sample}. The sampling timer keeps SAMPCON high after synchronization with AD12CLK for a programmed interval t_{sample}. The total sampling time is t_{sample} plus t_{sync} (see Figure 28-5).

The ADC12SHTx bits select the sampling time in 4× multiples of ADC12CLK. ADC12SHT0x selects the sampling time for ADC12MCTL0 to ADC12MCTL7. ADC12SHT1x selects the sampling time for ADC12MCTL8 to ADC12MCTL15.

28.2.10 ADC12_A Interrupts

The ADC12_A has 18 interrupt sources:

- ADC12IFG0 to ADC12IFG15
- ADC12OV, ADC12MEMx overflow
- ADC12TOV, ADC12_A conversion time overflow

The ADC12IFGx bits are set when their corresponding ADC12MEMx memory register is loaded with a conversion result. An interrupt request is generated if the corresponding ADC12IEx bit and the GIE bit are set. The ADC12OV condition occurs when a conversion result is written to any ADC12MEMx before its previous conversion result was read. The ADC12TOV condition is generated when another sample-and-conversion is requested before the current conversion is completed. The DMA is triggered after the conversion in single-channel conversion mode or after the completion of a sequence of channel conversions in sequence-of-channels conversion mode.

28.2.10.1 ADC12IV, Interrupt Vector Generator

All ADC12_A interrupt sources are prioritized and combined to source a single interrupt vector. The interrupt vector register ADC12IV is used to determine which enabled ADC12_A interrupt source requested an interrupt.

The highest-priority enabled ADC12_A interrupt generates a number in the ADC12IV register (see register description). This number can be evaluated or added to the program counter (PC) to automatically enter the appropriate software routine. Disabled ADC12_A interrupts do not affect the ADC12IV value.

Any access, read or write, of the ADC12IV register automatically resets the ADC12OV condition or the ADC12TOV condition if either was the highest-pending interrupt. Neither interrupt condition has an accessible interrupt flag. The ADC12IFGx flags are not reset by an ADC12IV access. ADC12IFGx bits are reset automatically by accessing their associated ADC12MEMx register or may be reset with software.

If another interrupt is pending after servicing of an interrupt, another interrupt is generated. For example, if the ADC12OV and ADC12IFG3 interrupts are pending when the interrupt service routine accesses the ADC12IV register, the ADC12OV interrupt condition is reset automatically. After the RETI instruction of the interrupt service routine is executed, the ADC12IFG3 generates another interrupt.

28.3.1 ADC12CTL0 Register

ADC12_A Control Register 0

Figure 28-13. ADC12CTL0 Register

15	14	13	12	11	10	9	8
ADC12SHT1x				ADC12SHT0x			
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC12MSC	ADC12REF2_5V	ADC12REFON	ADC12ON	ADC12OVIE	ADC12TOVIE	ADC12ENC	ADC12SC
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ADC12ENC = 0

Table 28-4. ADC12CTL0 Register Description

Bit	Field	Type	Reset	Description
15-12	ADC12SHT1x	RW	0h	ADC12_A sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM8 to ADC12MEM15.
11-8	ADC12SHT0x	RW	0h	ADC12_A sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM0 to ADC12MEM7. 0000b = 4 ADC12CLK cycles 0001b = 8 ADC12CLK cycles 0010b = 16 ADC12CLK cycles 0011b = 32 ADC12CLK cycles 0100b = 64 ADC12CLK cycles 0101b = 96 ADC12CLK cycles 0110b = 128 ADC12CLK cycles 0111b = 192 ADC12CLK cycles 1000b = 256 ADC12CLK cycles 1001b = 384 ADC12CLK cycles 1010b = 512 ADC12CLK cycles 1011b = 768 ADC12CLK cycles 1100b = 1024 ADC12CLK cycles 1101b = 1024 ADC12CLK cycles 1110b = 1024 ADC12CLK cycles 1111b = 1024 ADC12CLK cycles
7	ADC12MSC	RW	0h	ADC12_A multiple sample and conversion. Valid only for sequence or repeated modes. 0b = The sampling timer requires a rising edge of the SHI signal to trigger each sample-and-convert. 1b = The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed.
6	ADC12REF2_5V	RW	0h	ADC12_A reference generator voltage. ADC12REFON must also be set. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = 1.5 V 1b = 2.5 V
5	ADC12REFON	RW	0h	ADC12_A reference generator on. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = Reference off 1b = Reference on
4	ADC12ON	RW	0h	ADC12_A on 0b = ADC12_A off 1b = ADC12_A on

Table 28-4. ADC12CTL0 Register Description (continued)

Bit	Field	Type	Reset	Description
3	ADC12OVIE	RW	0h	ADC12MEMx overflow-interrupt enable. The GIE bit must also be set to enable the interrupt. 0b = Overflow interrupt disabled 1b = Overflow interrupt enabled
2	ADC12TOVIE	RW	0h	ADC12_A conversion-time-overflow interrupt enable. The GIE bit must also be set to enable the interrupt. 0b = Conversion time overflow interrupt disabled 1b = Conversion time overflow interrupt enabled
1	ADC12ENC	RW	0h	ADC12_A enable conversion 0b = ADC12_A disabled 1b = ADC12_A enabled
0	ADC12SC	RW	0h	ADC12_A start conversion. Software-controlled sample-and-conversion start. ADC12SC and ADC12ENC may be set together with one instruction. ADC12SC is reset automatically. 0b = No sample-and-conversion-start 1b = Start sample-and-conversion

28.3.2 ADC12CTL1 Register

ADC12_A Control Register 1

Figure 28-14. ADC12CTL1 Register

15	14	13	12	11	10	9	8
ADC12CSTARTADDx				ADC12SHSx		ADC12SHP	ADC12ISSH
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
ADC12DIVx			ADC12SSELx		ADC12CONSEQx		ADC12BUSY
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-(0)

Can be modified only when ADC12ENC = 0

Table 28-5. ADC12CTL1 Register Description

Bit	Field	Type	Reset	Description
15-12	ADC12CSTARTADDx	RW	0h	ADC12_A conversion start address. These bits select which ADC12_A conversion-memory register is used for a single conversion or for the first conversion in a sequence. The value of CSTARTADDx is 0 to 0Fh, corresponding to ADC12MEM0 to ADC12MEM15.
11-10	ADC12SHSx	RW	0h	ADC12_A sample-and-hold source select 00b = ADC12SC bit 01b = Timer source (see device-specific data sheet for exact timer and locations) 10b = Timer source (see device-specific data sheet for exact timer and locations) 11b = Timer source (see device-specific data sheet for exact timer and locations)
9	ADC12SHP	RW	0h	ADC12_A sample-and-hold pulse-mode select. This bit selects the source of the sampling signal (SAMPCON) to be either the output of the sampling timer or the sample-input signal directly. 0b = SAMPCON signal is sourced from the sample-input signal. 1b = SAMPCON signal is sourced from the sampling timer.
8	ADC12ISSH	RW	0h	ADC12_A invert signal sample-and-hold 0b = The sample-input signal is not inverted. 1b = The sample-input signal is inverted.
7-5	ADC12DIVx	RW	0h	ADC12_A clock divider 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b = Divide by 5 101b = Divide by 6 110b = Divide by 7 111b = Divide by 8
4-3	ADC12SSELx	RW	0h	ADC12_A clock source select 00b = ADC12OSC (MODCLK) 01b = ACLK 10b = MCLK 11b = SMCLK
2-1	ADC12CONSEQx	RW	0h	ADC12_A conversion sequence mode select 00b = Single-channel, single-conversion 01b = Sequence-of-channels 10b = Repeat-single-channel 11b = Repeat-sequence-of-channels
0	ADC12BUSY	R	0h	ADC12_A busy. This bit indicates an active sample or conversion operation. 0b = No operation is active. 1b = A sequence, sample, or conversion is active.

28.3.3 ADC12CTL2 Register

ADC12_A Control Register 2

Figure 28-15. ADC12CTL2 Register

15	14	13	12	11	10	9	8
Reserved							ADC12PDIV
r-0	r-0	r-0	r-0	r-0	r-0	r-0	rw-0

7	6	5	4	3	2	1	0
ADC12TCOFF	Reserved	ADC12RES		ADC12DF	ADC12SR	ADC12REFOUT	ADC12REFBURST
rw-(0)	r-0	rw-(1)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ADC12ENC = 0

Table 28-6. ADC12CTL2 Register Description

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0h	Reserved. Always reads as 0.
8	ADC12PDIV	RW	0h	ADC12_A predivider. This bit predivides the selected ADC12_A clock source. 0b = Predivide by 1 1b = Predivide by 4
7	ADC12TCOFF	RW	0h	ADC12_A temperature sensor off. If the bit is set, the temperature sensor turned off. This is used to save power. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = Temperature sensor on 1b = Temperature sensor off
6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	ADC12RES	RW	2h	ADC12_A resolution. This bit defines the conversion result resolution. 00b = 8 bit (9 clock cycle conversion time) 01b = 10 bit (11 clock cycle conversion time) 10b = 12 bit (13 clock cycle conversion time) 11b = Reserved
3	ADC12DF	RW	0h	ADC12_A data read-back format. Data is always stored in the binary unsigned format. 0b = Binary unsigned. Theoretically, the analog input voltage -VREF results in 0000h, the analog input voltage +VREF results in 0FFFh. 1b = Signed binary (twos complement), left aligned. Theoretically, the analog input voltage -VREF results in 8000h, the analog input voltage +VREF results in 7FF0h.
2	ADC12SR	RW	0h	ADC12_A sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC12SR reduces the current consumption of the reference buffer. 0b = Reference buffer supports up to approximately 200 ksps. 1b = Reference buffer supports up to approximately 50 ksps.
1	ADC12REFOUT	RW	0h	Reference output. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = Reference output off 1b = Reference output on
0	ADC12REFBURST	RW	0h	Reference burst 0b = Reference buffer on continuously 1b = Reference buffer on only during sample-and-conversion

28.3.4 ADC12MEMx Register

ADC12_A Conversion Memory Register

Figure 28-16. ADC12MEMx Register

15	14	13	12	11	10	9	8
Conversion Results							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Conversion Results							
rw	rw	rw	rw	rw	rw	rw	rw

Table 28-7. ADC12MEMx Register Description

Bit	Field	Type	Reset	Description
15-0	Conversion Results	RW	undefined	Binary unsigned format: This data format is used if ADC12DF = 0. The 12-bit conversion results are right justified. Bit 11 is the MSB. Bits 15–12 are 0 in 12-bit mode, bits 15–10 are 0 in 10-bit mode, and bits 15–8 are 0 in 8-bit mode. Writing to the conversion memory registers corrupts the results. Twos-complement format: This data format is used if ADC12DF = 1. The 12-bit conversion results are left justified, twos-complement format. Bit 15 is the MSB. Bits 3–0 are 0 in 12-bit mode, bits 5–0 are 0 in 10-bit mode, and bits 7–0 are 0 in 8-bit mode. The data is stored in the right-justified format and is converted to the left-justified twos-complement format during read back.

28.3.5 ADC12MCTLx Register

ADC12_A Conversion Memory Control Register

Figure 28-17. ADC12MCTLx Register

7	6	5	4	3	2	1	0
ADC12EOS	ADC12SREFx			ADC12INCHx			
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when ADC12ENC = 0

Table 28-8. ADC12MCTLx Register Description

Bit	Field	Type	Reset	Description
7	ADC12EOS	RW	0h	End of sequence. Indicates the last conversion in a sequence. 0b = Not end of sequence 1b = End of sequence
6-4	ADC12SREFx	RW	0h	Select reference 000b = V(R+) = AVCC and V(R-) = AVSS 001b = V(R+) = VREF+ and V(R-) = AVSS 010b = V(R+) = VeREF+ and V(R-) = AVSS 011b = V(R+) = VeREF+ and V(R-) = AVSS 100b = V(R+) = AVCC and V(R-) = VREF-/VeREF- 101b = V(R+) = VREF+ and V(R-) = VREF-/VeREF- 110b = V(R+) = VeREF+ and V(R-) = VREF-/VeREF- 111b = V(R+) = VeREF+ and V(R-) = VREF-/VeREF-
3-0	ADC12INCHx	RW	0h	Input channel select 0000b = A0 0001b = A1 0010b = A2 0011b = A3 0100b = A4 0101b = A5 0110b = A6 0111b = A7 1000b = VeREF+ 1001b = VREF-/VeREF- 1010b = Temperature diode 1011b = (AVCC – AVSS) / 2 1100b = A12. On devices with the Battery Backup System, VBAT can be measured internally by the ADC. 1101b = A13 1110b = A14 1111b = A15

28.3.6 ADC12IE Register

ADC12_A Interrupt Enable Register

Figure 28-18. ADC12IE Register

15	14	13	12	11	10	9	8
ADC12IE15	ADC12IE14	ADC12IE13	ADC12IE12	ADC12IE11	ADC12IE10	ADC12IE9	ADC12IE8
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
ADC12IE7	ADC12IE6	ADC12IE5	ADC12IE4	ADC12IE3	ADC12IE2	ADC12IE1	ADC12IE0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Table 28-9. ADC12IE Register Description

Bit	Field	Type	Reset	Description
15	ADC12IE15	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG15 bit. 0b = Interrupt disabled 1b = Interrupt enabled
14	ADC12IE14	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG14 bit. 0b = Interrupt disabled 1b = Interrupt enabled
13	ADC12IE13	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG13 bit. 0b = Interrupt disabled 1b = Interrupt enabled
12	ADC12IE12	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG12 bit. 0b = Interrupt disabled 1b = Interrupt enabled
11	ADC12IE11	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG11 bit. 0b = Interrupt disabled 1b = Interrupt enabled
10	ADC12IE10	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG10 bit. 0b = Interrupt disabled 1b = Interrupt enabled
9	ADC12IE9	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG9 bit. 0b = Interrupt disabled 1b = Interrupt enabled
8	ADC12IE8	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG8 bit. 0b = Interrupt disabled 1b = Interrupt enabled
7	ADC12IE7	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG7 bit. 0b = Interrupt disabled 1b = Interrupt enabled
6	ADC12IE6	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG6 bit. 0b = Interrupt disabled 1b = Interrupt enabled

Table 28-9. ADC12IE Register Description (continued)

Bit	Field	Type	Reset	Description
5	ADC12IE5	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG5 bit. 0b = Interrupt disabled 1b = Interrupt enabled
4	ADC12IE4	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG4 bit. 0b = Interrupt disabled 1b = Interrupt enabled
3	ADC12IE3	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG3 bit. 0b = Interrupt disabled 1b = Interrupt enabled
2	ADC12IE2	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG2 bit. 0b = Interrupt disabled 1b = Interrupt enabled
1	ADC12IE1	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG1 bit. 0b = Interrupt disabled 1b = Interrupt enabled
0	ADC12IE0	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG0 bit. 0b = Interrupt disabled 1b = Interrupt enabled

28.3.7 ADC12IFG Register

ADC12_A Interrupt Flag Register

Figure 28-19. ADC12IFG Register

15	14	13	12	11	10	9	8
ADC12IFG15	ADC12IFG14	ADC12IFG13	ADC12IFG12	ADC12IFG11	ADC12IFG10	ADC12IFG9	ADC12IFG8
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC12IFG7	ADC12IFG6	ADC12IFG5	ADC12IFG4	ADC12IFG3	ADC12IFG2	ADC12IFG1	ADC12IFG0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Table 28-10. ADC12IFG Register Description

Bit	Field	Type	Reset	Description
15	ADC12IFG15	RW	0h	ADC12MEM15 interrupt flag. This bit is set when ADC12MEM15 is loaded with a conversion result. This bit is reset if the ADC12MEM15 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
14	ADC12IFG14	RW	0h	ADC12MEM14 interrupt flag. This bit is set when ADC12MEM14 is loaded with a conversion result. This bit is reset if the ADC12MEM14 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
13	ADC12IFG13	RW	0h	ADC12MEM13 interrupt flag. This bit is set when ADC12MEM13 is loaded with a conversion result. This bit is reset if the ADC12MEM13 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
12	ADC12IFG12	RW	0h	ADC12MEM12 interrupt flag. This bit is set when ADC12MEM12 is loaded with a conversion result. This bit is reset if the ADC12MEM12 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
11	ADC12IFG11	RW	0h	ADC12MEM11 interrupt flag. This bit is set when ADC12MEM11 is loaded with a conversion result. This bit is reset if the ADC12MEM11 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
10	ADC12IFG10	RW	0h	ADC12MEM10 interrupt flag. This bit is set when ADC12MEM10 is loaded with a conversion result. This bit is reset if the ADC12MEM10 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
9	ADC12IFG9	RW	0h	ADC12MEM9 interrupt flag. This bit is set when ADC12MEM9 is loaded with a conversion result. This bit is reset if the ADC12MEM9 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
8	ADC12IFG8	RW	0h	ADC12MEM8 interrupt flag. This bit is set when ADC12MEM8 is loaded with a conversion result. This bit is reset if the ADC12MEM8 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending

LM76 ±0.5°C, ±1°C, 12-Bit + Sign Digital Temperature Sensor and Thermal Window Comparator with Two-Wire Interface

Check for Samples: LM76

FEATURES

- **Window Comparison Simplifies Design of ACPI Compatible Temperature Monitoring and Control.**
- **Serial Bus Interface**
- **Separate Open-Drain Outputs for Interrupt and Critical Temperature Shutdown**
- **Shutdown Mode to Minimize Power Consumption**
- **Up to 4 LM76s can be Connected to a Single Bus**
- **12-bit + Sign Output; Full-scale Reading of Over 127°C**

KEY SPECIFICATIONS

- **Supply Voltage 5.0V**
- **Supply Current**
  - **Operating**
    - **250 µA (typ)**
    - **450 µA (max)**
  - **Shutdown**
    - **8 µA (max)**
- **Temperature +25ºC ±0.5ºC (max)**
  - **Accuracy**
    - **–10ºC to +45ºC ±10°C (max)**
    - **70°C to 100°C ±1.0°C (max)**
- **Resolution 0.0625°C**

APPLICATIONS

- **System Thermal Management**
- **Personal Computers**
- **Office Electronics**
- **HVAC**

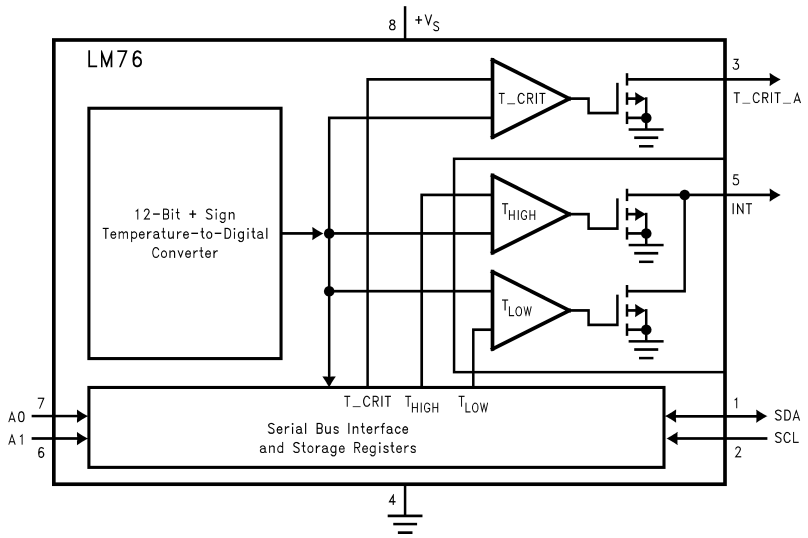
DESCRIPTION

The LM76 is a digital temperature sensor and thermal window comparator with an I^2C Serial Bus interface with an accuracy of ±1°C. This accuracy for the LM76CHM is specified for a −10°C to 45°C temperature range. The LM76CHM is specified with an accuracy ±0.5°C at 25°C. The window-comparator architecture of the LM76 eases the design of temperature control systems conforming to the ACPI (Advanced Configuration and Power Interface) specification for personal computers. The open-drain Interrupt (INT) output becomes active whenever temperature goes outside a programmable window, while a separate Critical Temperature Alarm (T_CRIT_A) output becomes active when the temperature exceeds a programmable critical limit. The INT output can operate in either a comparator or event mode, while the T_CRIT_A output operates in comparator mode only.

The host can program both the upper and lower limits of the window as well as the critical temperature limit. Programmable hysterisis as well as a fault queue are available to minimize false tripping. Two pins (A0, A1) are available for address selection. The sensor powers up with default thresholds of 2°C T_{HYST}, 10°C T_{LOW}, 64°C T_{HIGH}, and 80°C T_CRIT.

The LM76's 5.0V supply voltage, Serial Bus interface, 12-bit + sign output, and full-scale range of over 127°C make it ideal for a wide range of applications. These include thermal management and protection applications in personal computers, electronic test equipment, office electronics and bio-medical applications.

Simplified Block Diagram



Connection Diagram

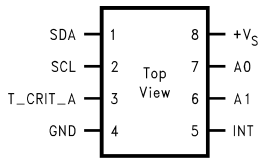


Figure 1. SOIC-8
LM76 See Package Number D

PIN DESCRIPTIONS

Label	Pin #	Function	Typical Connection
SDA	1	Serial Bi-Directional Data Line, Open Drain Output, CMOS Logic Level	Pull Up Resistor, Controller I^2C Data Line
SCL	2	Serial Bus Clock Input, CMOS Logic Level	From Controller I^2C Clock Line
T_CRIT_A	3	Critical Temperature Alarm, Open Drain Output	Pull Up Resistor, Controller Interrupt Line or System Hardware Shutdown
GND	4	Power Supply Ground	Ground
INT	5	Interrupt, Open Drain Output	Pull Up Resistor, Controller Interrupt Line
A0–A1	7, 6	User-Set Address Inputs, TTL Logic Level	Ground (Low, “0”) or $+V_S$ (High, “1”)
$+V_S$	8	Positive Supply Voltage Input	DC Voltage from 3.3V power supply or 5V.

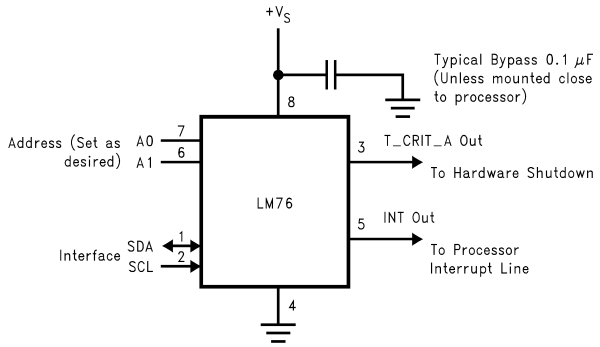


Figure 2. Typical Application

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

Supply Voltage		−0.3V to 6.5V
Voltage at any Pin		−0.3V to ($+V_S$ + 0.3V)
Input Current at any Pin		5mA
Package Input Current[2]		20mA
T_CRIT_A and INT Output Sink Current		10mA
T_CRIT_A and INT Output Voltage		6.5V
Storage Temperature		−65°C to +125°C
Soldering Information, Lead Temperature		
SOIC Package[3]	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C
ESD Susceptibility [4]	Human Body Model	3000V
	Machine Model	250V

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) When the input voltage (V_I) at any pin exceeds the power supplies (V_I < GND or V_I > $+V_S$) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5 mA to four.
(3) See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current Texas Instruments Linear Data Book for other methods of soldering surface mount devices.
(4) Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.

Operating Ratings[1][2]

Operating Temperature Range	−55°C to +150°C
Specified Temperature Range[3]	T_{MIN} to T_{MAX}
LM76CHM-5	−20°C to +85°C
Supply Voltage Range ($+V_S$)[4]	+4.5V to +5.5V

(1) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.
(2) LM76 θ_{JA} (thermal resistance, junction-to-ambient) when attached to a printed circuit board with 2 oz. foil is 200°C/W.
(3) While the LM76 has a full-scale-range in excess of 128°C, prolonged operation at temperatures above 125°C is not recommended.
(4) The LM76 will operate properly over the $+V_S$ supply voltage range of 3V to 5.5V for the LM76CNM-3 and the LM76CHM-5. The LM76CNM-3 is tested and specified for rated accuracy at the nominal supply voltage of 3.3V. Accuracy of the LM76CNM-3 will degrade 0.2°C for a ±1% variation in $+V_S$ from the nominal value. The LM76CHM-5 is tested and specified for a rated accuracy at the nominal supply voltage of 5.0V. Accuracy of the LM76CHM-5 will degrade 0.08°C for a ±1% variation in $+V_S$ from the nominal value.

Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for $+V_S$ = +5.0 Vdc ±10% for the LM76CHM-5.[1]. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = +25°C, unless otherwise noted.

Parameter	Conditions	Typical[2]	LM76CNM-3 Limits[3]	LM76CHM-5 Limits[3]	Units (Limit)
Accuracy[1]	T_A = +70°C to +100°C		**±1.0**		
	T_A = −20°C to +85°C for LM76CHM-5	±1.5			
	T_A = −10°C to +45°C			**±1.0**	
	T_A = +25°C			±0.5	
Resolution	See[4]	13 0.0625			Bits °C
Temperature Conversion Time	See[5]	400	**500**	**1000**	ms
Quiescent Current	I^2C Inactive	0.25			mA
	I^2C Active	0.25	**0.5**	**0.45**	mA (max)
	Shutdown Mode:	5			µA
			12	**18**	µA (max)
	T_A = +85°C		8		µA (max)
	T_A = +25°C			12	µA (max)
T_{HYST} Default Temperature	See[6][7]	2			°C
T_{LOW} Default Temperature	See[7]	10			°C
T_{HIGH} Default Temperature	See[7]	64			°C
T_{CRIT} Default Temperature	See[7]	80			°C

(1) The LM76 will operate properly over the $+V_S$ supply voltage range of 3V to 5.5V for the LM76CNM-3 and the LM76CHM-5. The LM76CNM-3 is tested and specified for rated accuracy at the nominal supply voltage of 3.3V. Accuracy of the LM76CNM-3 will degrade 0.2°C for a ±1% variation in $+V_S$ from the nominal value. The LM76CHM-5 is tested and specified for a rated accuracy at the nominal supply voltage of 5.0V. Accuracy of the LM76CHM-5 will degrade 0.08°C for a ±1% variation in $+V_S$ from the nominal value.
(2) Typicals are at T_A = 25°C and represent most likely parametric norm.
(3) Limits are ensured to AOQL (Average Outgoing Quality Level).
(4) 12 bits + sign, two's complement
(5) This specification is provided only to indicate how often temperature data is updated. The LM76 can be read at any time without regard to conversion state (and will yield last conversion result). If a conversion is in process it will be interrupted and restarted after the end of the read.
(6) Hysteresis value adds to the T_{LOW} setpoint value (e.g.: if T_{LOW} setpoint = 10°C, and hysteresis = 2°C, then actual hysteresis point is 10+2 = 12°C); and subtracts from the T_{HIGH} and T_CRIT setpoints (e.g.: if T_{HIGH} setpoint = 64°C, and hysteresis = 2°C, then actual hysteresis point is 64−2 = 62°C). For a detailed discussion of the function of hysteresis refer to TEMPERATURE COMPARISON, and Figure 6.
(7) Default values set at power up.

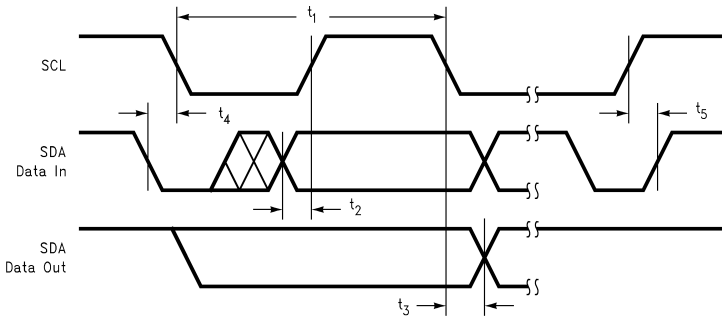


Figure 3. Timing Diagram

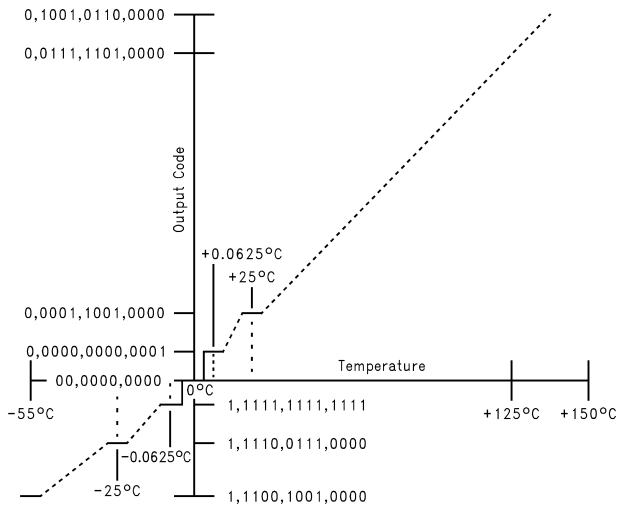


Figure 4. Temperature-to-Digital Transfer Function (Non-linear scale for clarity)

DEFAULT SETTINGS

The LM76 always powers up in a known state. LM76 power up default conditions are:

1. Comparator Interrupt Mode
2. T_{LOW} set to 10°C
3. T_{HIGH} set to 64°C
4. T_CRIT set to 80°C
5. T_{HYST} set to 2°C
6. INT and T_CRIT_A active low
7. Pointer set to “00”; Temperature Register

The LM76 registers will always reset to these default values when the power supply voltage is brought up from zero volts as the supply crosses the voltage level plotted in the following curve. The LM76 registers will reset again when the power supply drops below the voltage plotted in this curve.

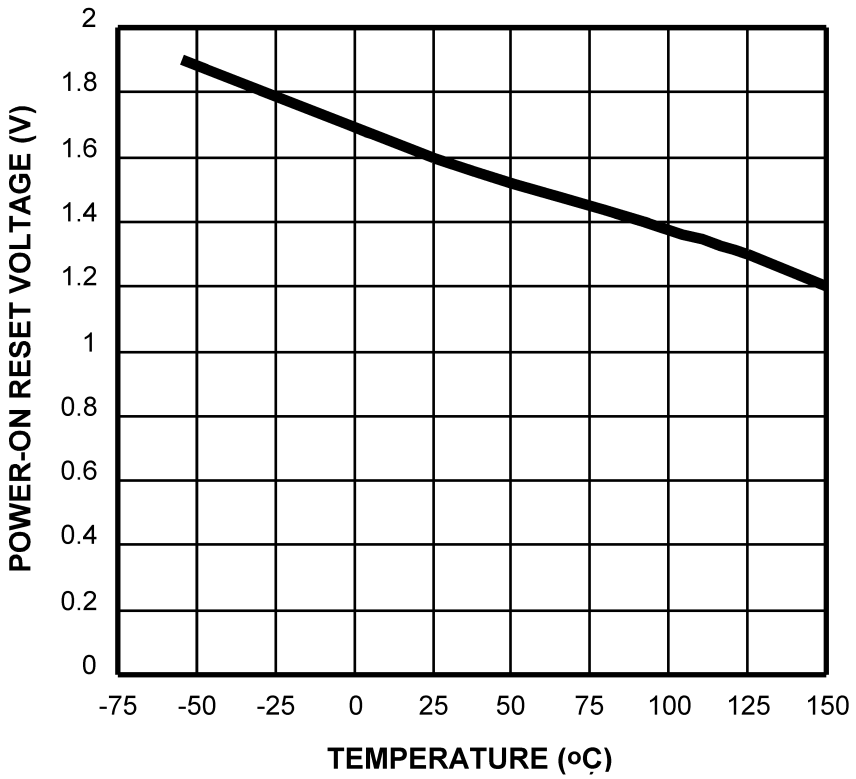


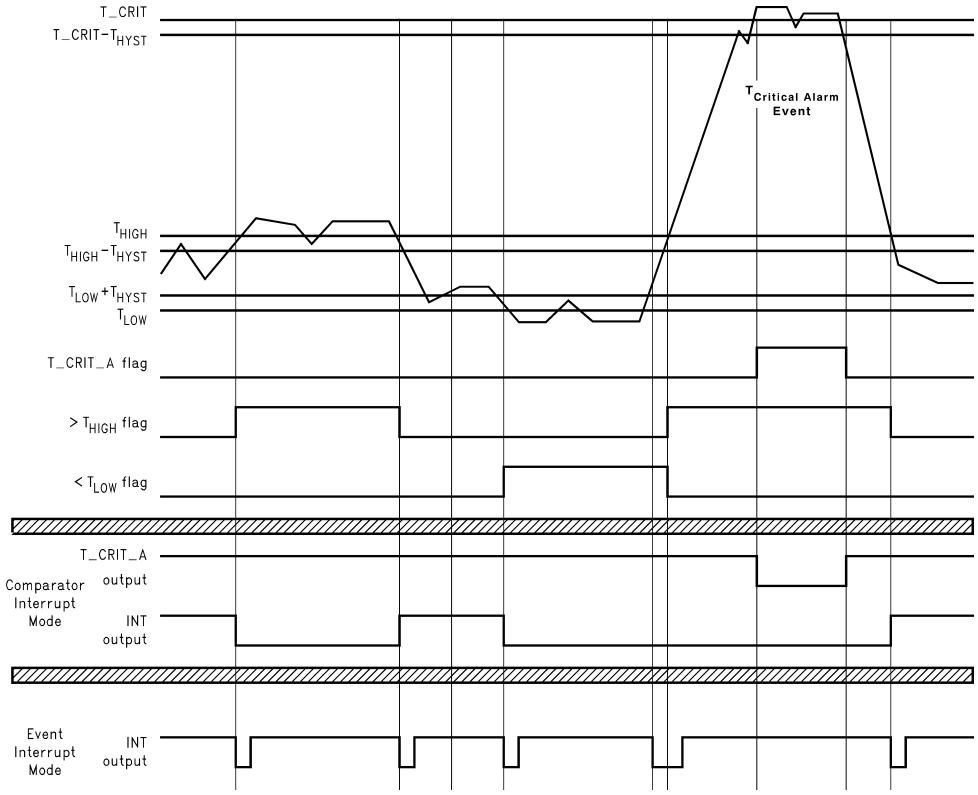
Figure 5. Average Power on Reset Voltage vs Temperature

SERIAL BUS INTERFACE

The LM76 operates as a slave on the Serial Bus, so the SCL line is an input (no clock is generated by the LM76) and the SDA line is a bi-directional serial data line. According to Serial Bus specifications, the LM76 has a 7-bit slave address. The five most significant bits of the slave address are hard wired inside the LM76 and are “10010”. The two least significant bits of the address are assigned to pins A1–A0, and are set by connecting these pins to ground for a low, (0); or to $+V_S$ for a high, (1).

Therefore, the complete slave address is:

1	0	0	1	0	A1	A0
MSB						LSB



Event Interrupt mode is drawn as if the user is reading the part. If the user doesn't read, the outputs would go low and stay that way until the LM76 is read.

Figure 6. Temperature Response Diagram

TEMPERATURE DATA FORMAT

Temperature data can be read from the Temperature and Set Point registers; and written to the Set Point registers. Temperature data can be read at any time, although reading faster than the conversion time of the LM76 will prevent data from being updated. Temperature data is represented by a 13-bit, two's complement word with an LSB (Least Significant Bit) equal to 0.0625°C:

Temperature	Digital Output	
	Binary	Hex
+130°C	0 1000 0 010 0000	08 20h
+125°C	0 0111 1101 0000	07 D0h
+80°C	0 0101 1010 0000	05 90h
+64°C	0 0100 0000 0000	04 00h
+25°C	0 0001 1001 0000	01 90h
+10°C	0 0000 1010 0000	00 A0h
+2°C	0 0000 0010 0000	00 20h
+0.0625°C	0 0000 0000 0001	00 01h
0°C	00 0000 0000	00 00h
−0.0625°C	1 1111 1111 1111	1F FFh
−25°C	1 1110 0111 0000	1E 70h
−55°C	1 1100 1001 0000	1C 90h

The first data byte is the most significant byte with most significant bit first, permitting only as much data as necessary to be read to determine the temperature condition. For instance, if the first four bits of the temperature data indicates a critical condition, the host processor could immediately take action to remedy the excessive temperature. At the end of a read, the LM76 can accept either Acknowledge or No Acknowledge from the Master (No Acknowledge is typically used as a signal for the slave that the Master has read its last byte).

An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the LM76 to stop in a state where the SDA line is held low as shown in Figure 7. This can prevent any further bus communication until at least 9 additional clock cycles have occurred. Alternatively, the master can issue clock cycles until SDA goes high, at which time issuing a “Stop” condition will reset the LM76.

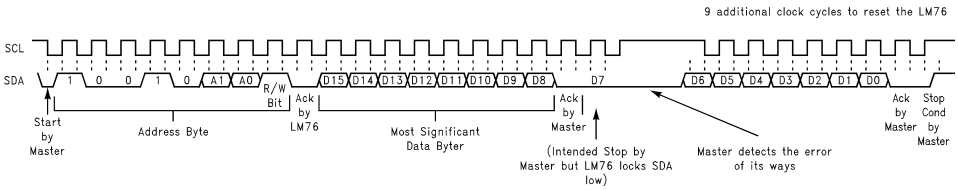


Figure 7. Inadvertent 8-Bit Read from 16-Bit Register where D7 is Zero (“0”)

POINTER REGISTER

(Selects which registers will be read from or written to):

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	Register Select		

P0–P2: Register Select:

P2	P1	P0	Register
0	0	0	Temperature (Read only) (Power-up default)-
0	0	1	Configuration (Read/Write)
0	1	0	T_{HYST} (Read/Write)
0	1	1	T_CRIT (Read/Write)
1	0	0	T_{LOW} (Read/Write)
1	0	1	T_{HIGH} (Read/Write)

P3–P7: Must be kept zero.

TEMPERATURE REGISTER

Table 1. (Read Only):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign	MSB	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CRIT	HIGH	LOW
													Status Bits		

D0–D2: Status Bits

D3–D15: Temperature Data. One LSB = 0.0625°C. Two's complement format.

CONFIGURATION REGISTER

Table 2. (Read/Write):

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Fault Queue	INT Polarity	T_CRIT_A Polarity	INT Mode	Shutdown

D0: Shutdown - When set to 1 the LM76 goes to low power shutdown mode. Power up default of “0”.

D1: Interrupt mode - 0 is Comparator Interrupt mode, 1 is Event Interrupt mode. Power up default of “0”.

D2, D3: T_CRIT_A and INT Polarity - 0 is active low, 1 is active high. Outputs are open-drain. Power up default of “0”

D4: Fault Queue - When set to 1 the Fault Queue is enabled, see FAULT QUEUE. Power up default of “0”.

D5–D7: These bits are used for production testing and must be kept zero for normal operation.

T_{HYST}, T_{LOW}, T_{HIGH} AND T_CRIT_A REGISTERS

Table 3. (Read/Write):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign	MSB	Bit 10	Bit 9	Bit 8	Bit7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	X	X	X

D0–D2: Undefined

D3–D15: T_{HYST}, T_{LOW}, T_{HIGH} or T_CRIT Trip Temperature Data. Power up default is T_{LOW} = 10°C, T_{HIGH} = 64°C, T_CRIT = 80°C, T_{HYST} = 2°C.

T_{HYST} is subtracted from T_{HIGH}, and T_CRIT, and added to T_{LOW}.

Avoid programming setpoints so close that their hysteresis values overlap. See CONFIGURATION REGISTER .

TEST CIRCUIT DIAGRAMS

I²C Timing Diagrams

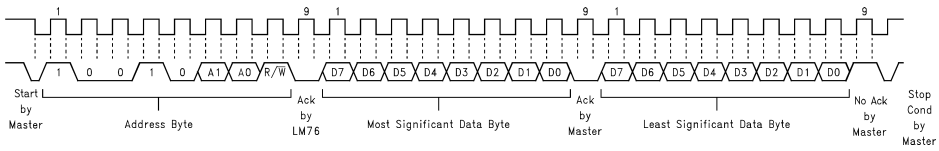


Figure 8. Typical 2-Byte Read From Preset Pointer Location Such as Temp or Comparison Registers

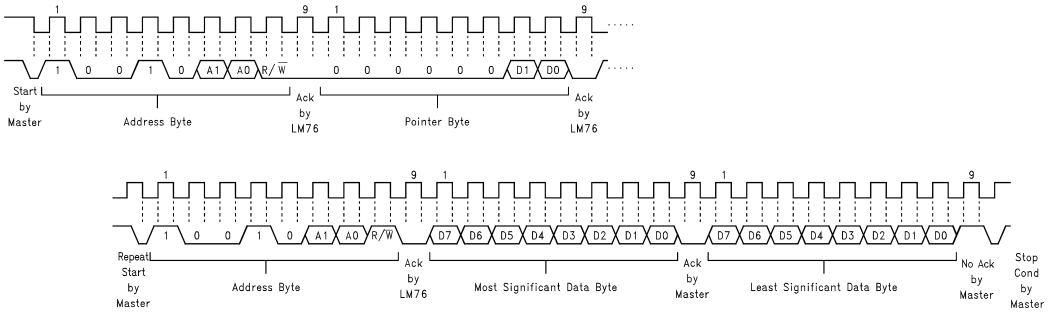


Figure 9. Typical Pointer Set Followed by Immediate Read for 2-Byte Register such as Temp or Comparison Registers

Typical Applications

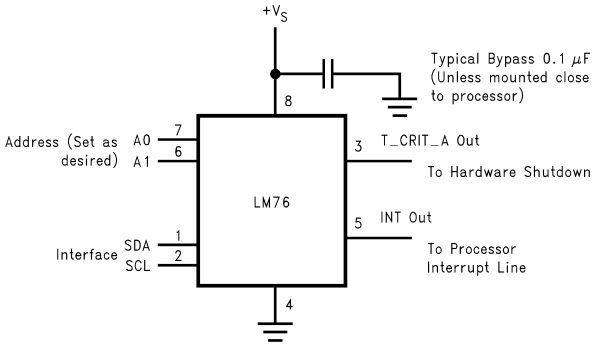


Figure 15. Typical Application

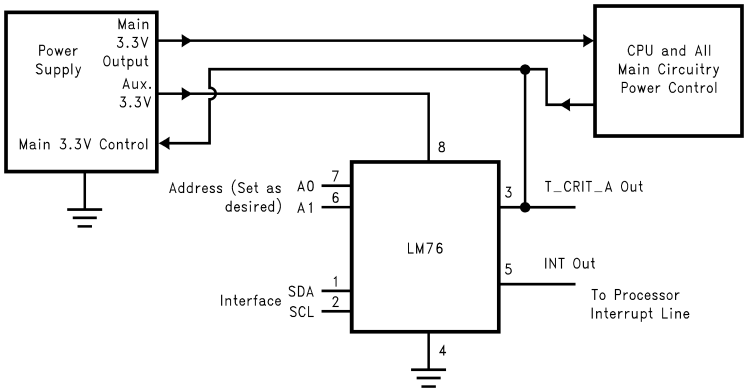


Figure 16. ACPI Compatible Terminal Alarm Shutdown

By powering the LM76 from auxiliary output of the power supply, a non-functioning overheated computer can be powered down to preserve as much of the system as possible.

LM35 Precision Centigrade Temperature Sensors

1 Features

- Calibrated Directly in Celsius (Centigrade)
- Linear + 10-mV/°C Scale Factor
- 0.5°C Ensured Accuracy (at 25°C)
- Rated for Full −55°C to 150°C Range
- Suitable for Remote Applications
- Low-Cost Due to Wafer-Level Trimming
- Operates from 4 V to 30 V
- Less than 60-µA Current Drain
- Low Self-Heating, 0.08°C in Still Air
- Non-Linearity Only ±¼°C Typical
- Low-Impedance Output, 0.1 Ω for 1-mA Load

2 Applications

- Power Supplies
- Battery Management
- HVAC
- Appliances

3 Description

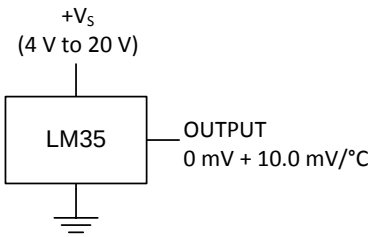
The LM35 series are precision integrated-circuit temperature devices with an output voltage linearly-proportional to the Centigrade temperature. The LM35 device has an advantage over linear temperature sensors calibrated in Kelvin, as the user is not required to subtract a large constant voltage from the output to obtain convenient Centigrade scaling. The LM35 device does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55°C to 150°C temperature range. Lower cost is assured by trimming and calibration at the wafer level. The low-output impedance, linear output, and precise inherent calibration of the LM35 device makes interfacing to readout or control circuitry especially easy. The device is used with single power supplies, or with plus and minus supplies. As the LM35 device draws only 60 µA from the supply, it has very low self-heating of less than 0.1°C in still air. The LM35 device is rated to operate over a −55°C to 150°C temperature range, while the LM35C device is rated for a −40°C to 110°C range (−10° with improved accuracy). The LM35-series devices are available packaged in hermetic TO transistor packages, while the LM35C, LM35CA, and LM35D devices are available in the plastic TO-92 transistor package. The LM35D device is available in an 8-lead surface-mount small-outline package and a plastic TO-220 package.

Device Information(1)

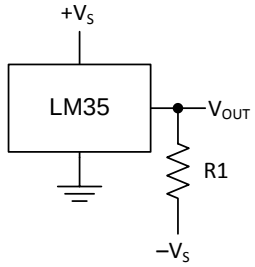
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM35	TO-CAN (3)	4.699 mm × 4.699 mm
	TO-92 (3)	4.30 mm × 4.30 mm
	SOIC (8)	4.90 mm × 3.91 mm
	TO-220 (3)	14.986 mm × 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Basic Centigrade Temperature Sensor (2°C to 150°C)



Full-Range Centigrade Temperature Sensor



Choose $R_1 = -V_S / 50\ \mu A$
V_{OUT} = 1500 mV at 150°C
V_{OUT} = 250 mV at 25°C
V_{OUT} = –550 mV at –55°C

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

		MIN	MAX	UNIT
Supply voltage		–0.2	35	V
Output voltage		–1	6	V
Output current			10	mA
Maximum Junction Temperature, $T_J$max			150	°C
Storage Temperature, T_{stg}	TO-CAN, TO-92 Package	–60	150	°C
	TO-220, SOIC Package	–65	150	

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Specified operating temperature: T_{MIN} to T_{MAX}	LM35, LM35A	–55	150	°C
	LM35C, LM35CA	–40	110	
	LM35D	0	100	
Supply Voltage (+V_S)		4	30	V

6.4 Thermal Information

THERMAL METRIC[1][2]		LM35				UNIT
		NDV	LP	D	NEB	
		3 PINS		8 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	400	180	220	90	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24	—	—	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For additional thermal resistance information, see *Typical Application*.

6.6 Electrical Characteristics: LM35A, LM35CA

Unless otherwise noted, these specifications apply: −55°C ≤ T_J ≤ 150°C for the LM35 and LM35A; −40°C ≤ T_J ≤ 110°C for the LM35C and LM35CA; and 0°C ≤ T_J ≤ 100°C for the LM35D. V_S = 5 Vdc and I_{LOAD} = 50 µA, in the circuit of Full-Range Centigrade Temperature Sensor. These specifications also apply from 2°C to T_{MAX} in the circuit of Figure 14.

PARAMETER	TEST CONDITIONS		LM35A			LM35CA			UNIT
			MIN	TYP	MAX	TYP	TYP	MAX	
Accuracy(1)	T_A = 25°C			±0.2			±0.2		°C
		Tested Limit(2)			±0.5			±0.5	
		Design Limit(3)							
	T_A = –10°C			±0.3			±0.3		
		Tested Limit(2)							
		Design Limit(3)						±1	
	T_A = T_{MAX}			±0.4			±0.4		
		Tested Limit(2)			±1			±1	
		Design Limit(3)							
	T_A = T_{MIN}			±0.4			±0.4		
		Tested Limit(2)			±1				
		Design Limit(3)						±1.5	
Nonlinearity(4)	T_{MIN} ≤ T_A ≤ T_{MAX}, –40°C ≤ T_J ≤ 125°C			±0.18			±0.15		°C
		Tested Limit(2)							
		Design Limit(3)			±0.35			±0.3	
Sensor gain (average slope)	T_{MIN} ≤ T_A ≤ T_{MAX}			10			10		mV/°C
		Tested Limit(2)			9.9				
		Design Limit(3)						9.9	
	–40°C ≤ T_J ≤ 125°C			10			10		
		Tested Limit(2)			10.1				
		Design Limit(3)						10.1	
Load regulation(5) 0 ≤ I_L ≤ 1 mA	T_A = 25°C			±0.4			±0.4		mV/mA
		Tested Limit(2)			±1			±1	
		Design Limit(3)							
	T_{MIN} ≤ T_A ≤ T_{MAX}, –40°C ≤ T_J ≤ 125°C			±0.5			±0.5		
		Tested Limit(2)							
		Design Limit(3)			±3			±3	
Line regulation(5)	T_A = 25°C			±0.01			±0.01		mV/V
		Tested Limit(2)			±0.05			±0.05	
		Design Limit(3)							
	4 V ≤ V_S ≤ 30 V, –40°C ≤ T_J ≤ 125°C			±0.02			±0.02		
		Tested Limit(2)							
		Design Limit(3)			±0.1			±0.1	

(1) Accuracy is defined as the error between the output voltage and 10 mv/°C times the case temperature of the device, at specified conditions of voltage, current, and temperature (expressed in °C).
(2) Tested Limits are ensured and 100% tested in production.
(3) Design Limits are ensured (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.
(4) Non-linearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the rated temperature range of the device.
(5) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Electrical Characteristics: LM35A, LM35CA (continued)

Unless otherwise noted, these specifications apply: −55°C ≤ T_J ≤ 150°C for the LM35 and LM35A; −40°C ≤ T_J ≤ 110°C for the LM35C and LM35CA; and 0°C ≤ T_J ≤ 100°C for the LM35D. V_S = 5 Vdc and I_{LOAD} = 50 µA, in the circuit of Full-Range Centigrade Temperature Sensor. These specifications also apply from 2°C to T_{MAX} in the circuit of Figure 14.

PARAMETER	TEST CONDITIONS		LM35A			LM35CA			UNIT
			MIN	TYP	MAX	TYP	TYP	MAX	
Quiescent current(6)	V_S = 5 V, 25°C			56			56		µA
		Tested Limit(2)			67			67	
		Design Limit(3)							
	V_S = 5 V, –40°C ≤ T_J ≤ 125°C			105			91		
		Tested Limit(2)							
		Design Limit(3)			131			114	
	V_S = 30 V, 25°C			56.2			56.2		
		Tested Limit(2)			68			68	
		Design Limit(3)							
	V_S = 30 V, –40°C ≤ T_J ≤ 125°C			105.5			91.5		
		Tested Limit(2)							
		Design Limit(3)			133			116	
Change of quiescent current(5)	4 V ≤ V_S ≤ 30 V, 25°C			0.2			0.2		µA
		Tested Limit(2)			1			1	
		Design Limit(3)							
	4 V ≤ V_S ≤ 30 V, –40°C ≤ T_J ≤ 125°C			0.5			0.5		
		Tested Limit(2)							
		Design Limit(3)			2			2	
Temperature coefficient of quiescent current	–40°C ≤ T_J ≤ 125°C			0.39			0.39		µA/°C
		Tested Limit(2)							
		Design Limit(3)			0.5			0.5	
Minimum temperature for rate accuracy	In circuit of Figure 14, I_L = 0			1.5			1.5		°C
		Tested Limit(2)							
		Design Limit(3)			2			2	
Long term stability	T_J = T_{MAX}, for 1000 hours			±0.08			±0.08		°C

(6) Quiescent current is defined in the circuit of Figure 14.

6.9 Typical Characteristics

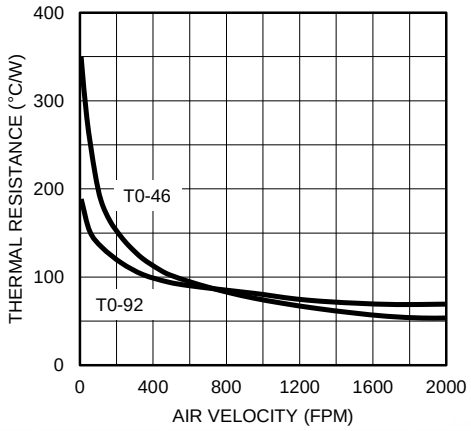


Figure 1. Thermal Resistance Junction To Air

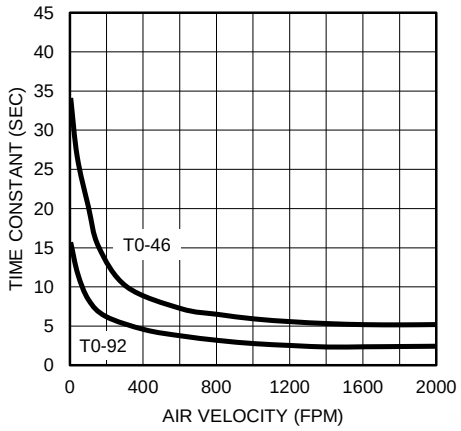


Figure 2. Thermal Time Constant

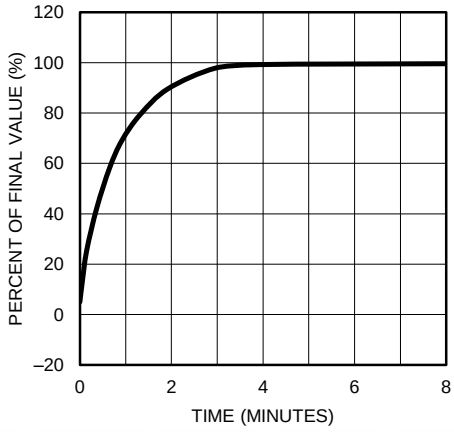


Figure 3. Thermal Response In Still Air

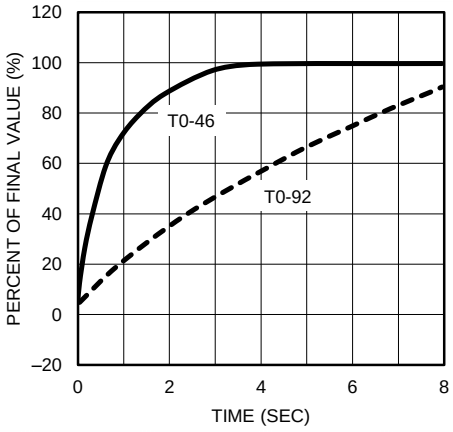


Figure 4. Thermal Response In Stirred Oil Bath

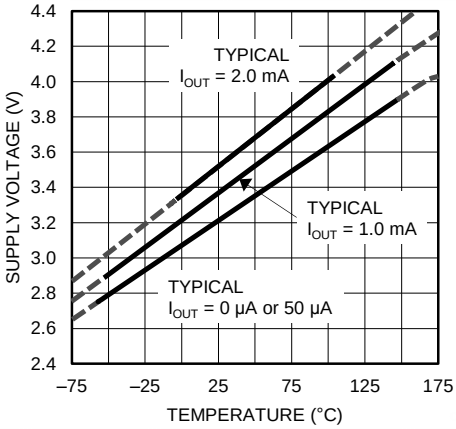


Figure 5. Minimum Supply Voltage vs Temperature

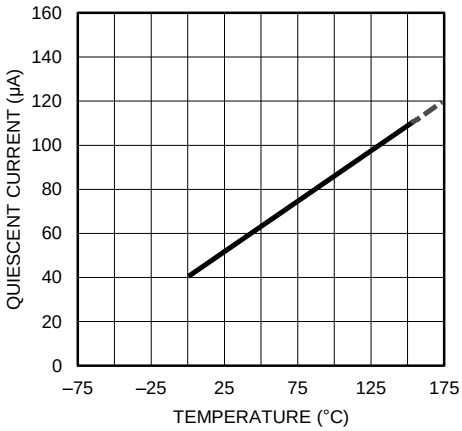


Figure 6. Quiescent Current vs Temperature (in Circuit of Figure 14)

Typical Characteristics (continued)

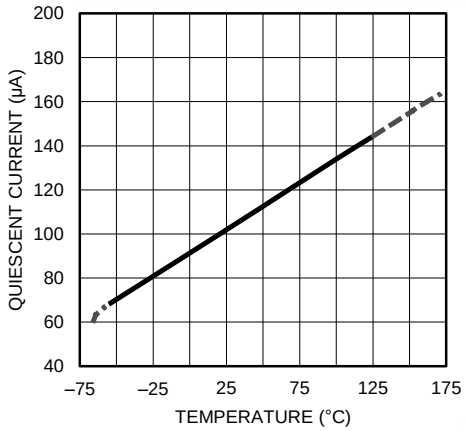


Figure 7. Quiescent Current vs Temperature (in Circuit of Full-Range Centigrade Temperature Sensor)

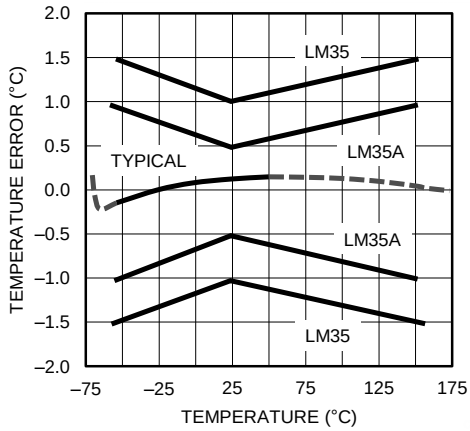


Figure 8. Accuracy vs Temperature (Ensured)

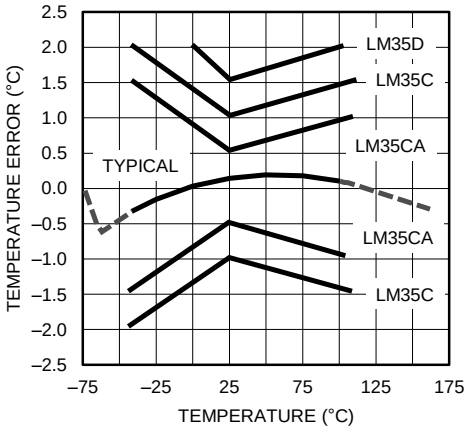


Figure 9. Accuracy vs Temperature (Ensured)

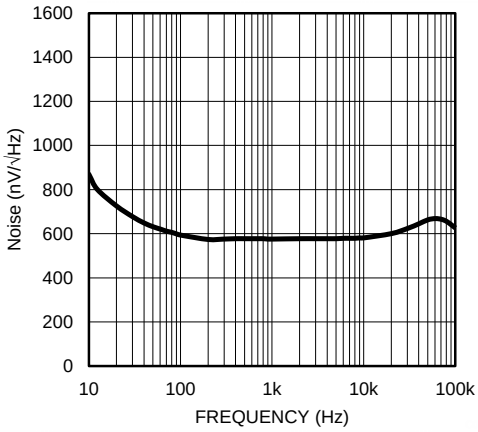


Figure 10. Noise Voltage

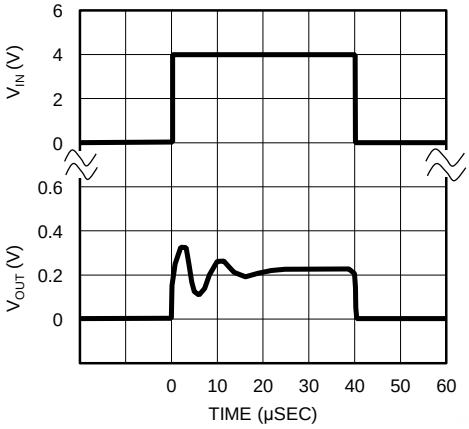


Figure 11. Start-Up Response

8.2 Typical Application

8.2.1 Basic Centigrade Temperature Sensor

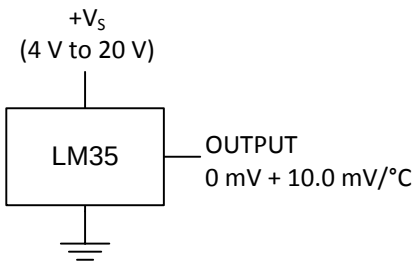


Figure 14. Basic Centigrade Temperature Sensor (2 °C to 150 °C)

8.2.1.1 Design Requirements

Table 1. Design Parameters

PARAMETER	VALUE
Accuracy at 25°C	±0.5°C
Accuracy from –55 °C to 150°C	±1°C
Temperature Slope	10 mV/°C

8.2.1.2 Detailed Design Procedure

Because the LM35 device is a simple temperature sensor that provides an analog output, design requirements related to layout are more important than electrical requirements. For a detailed description, refer to the *Layout*.

8.2.1.3 Application Curve

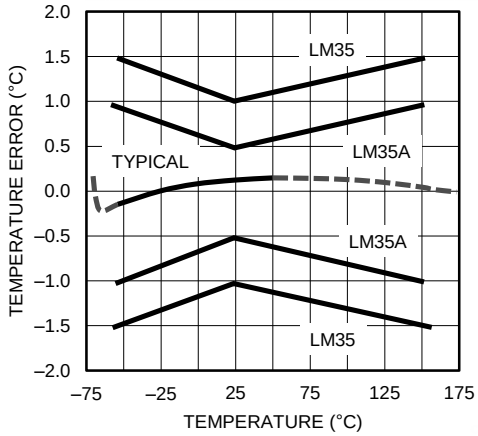


Figure 15. Accuracy vs Temperature (Ensured)

8.3 System Examples

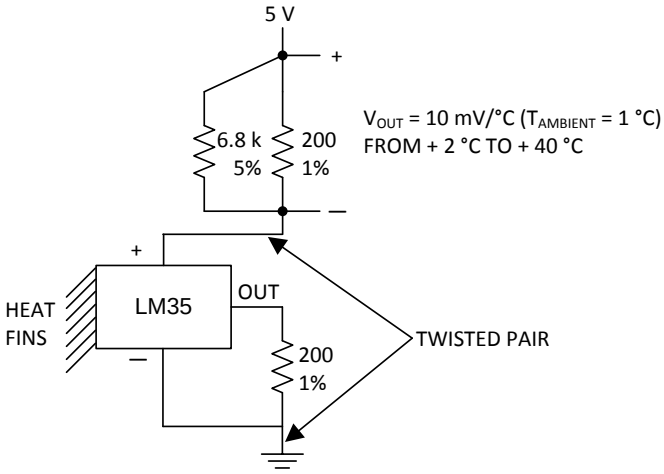


Figure 16. Two-Wire Remote Temperature Sensor (Grounded Sensor)

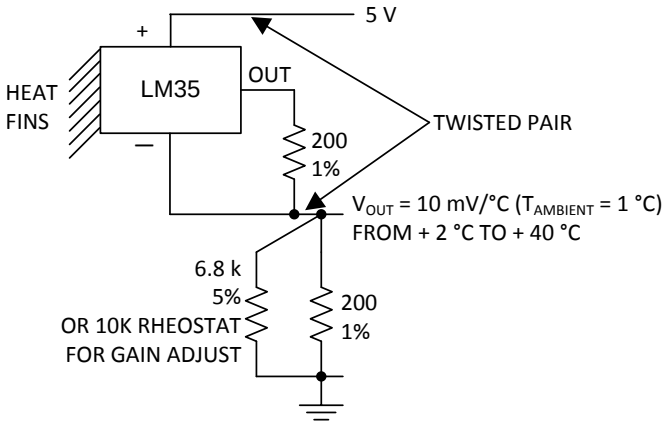


Figure 17. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

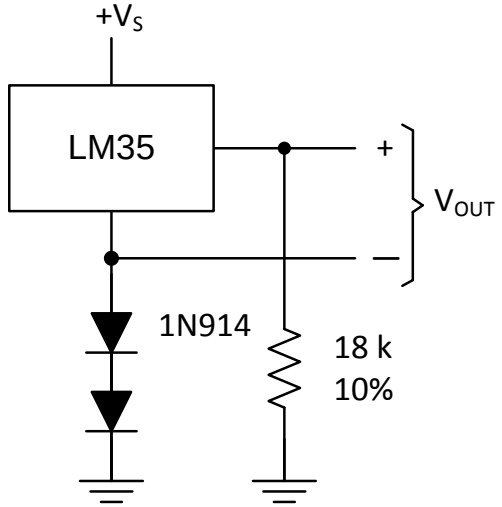


Figure 18. Temperature Sensor, Single Supply (−55° to +150°C)

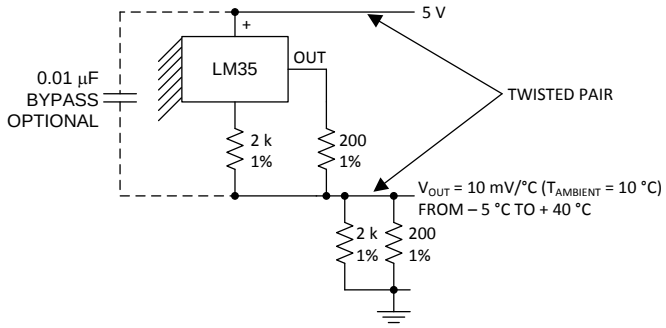


Figure 19. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

ROHM SEMICONDUCTOR

Datasheet

Temperature Sensor IC
Analog Output
BD1020HFV

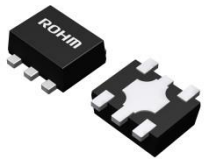
General Description
BD1020HFV is a low quiescent current (4µA) and high accuracy temperature sensor.
This IC has a linear response with respect to temperature.

Features
- Low Thermal Resistance (typically 187°C/W)
- ESD Rating 8kV (HBM)
- Excellent Ripple Rejection Characteristics

Applications
Cell Phone (RF Module, Battery Thermal Management), Audio Systems, Digital Still Camera, LCD, PDP,
Optical pick up module for DVD and BlueRay

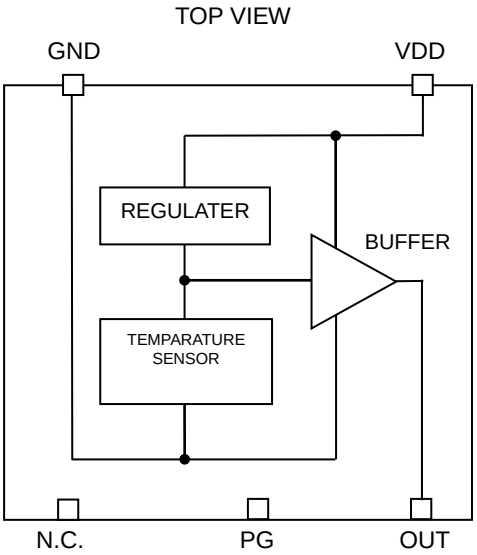
Key Specifications
- Operating Voltage Range: 2.4V to 5.5V
- High Accuracy: ±1.5°C(Max) @Ta=30°C
  ±2.5°C (Max) @Ta=-30°C, +100°C
- Temperature Sensitivity: -8.2 mV/°C (Typ)
- Quiescent Current: 4.0µA(Typ)
- Detection Temperature Range: -30°C to +100°C

Package W (Typ) x D (Typ) x H (Max)



HVSOF5
1.60mm x 1.60mm x 0.60mm

Block Diagram and Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function	Comment
1	N.C.	-	Please set to OPEN .
2	PG	Heat Condition	Please connect to Temperature Measurement part.
3	OUT	Output Voltage for is inversely proportional with temperature	-
4	VDD	Power Supply	-
5	GND	Ground	-

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	V_{DD}	-0.3 to +7.0 (Note 1)	V
Output Voltage	V_{OUT}	-0.3 to +V_{DD}+0.3	V
Output Current	I_{OUT}	±1	mA
Power Dissipation	Pd	0.53 (Note 2)	W
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) However, not exceeding Pd.
(Note 2) When mounted on ROHM standard board, derate by 5.36mW/°C for Ta higher than 25 °C.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	2.40	3.00	5.50	V
Operation Temperature	Topr	-30	-	+100	°C

Electrical Characteristics

(Unless otherwise specified, V_{DD}=3.0V, Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Accuracy	Tacc	-	-	±1.5	°C	Ta = 30°C
		-	-	±2.5		Ta = 100°C
		-	-	±2.5		Ta = -30°C
Temperature Sensitivity	V_{SE}	-8.4	-8.2	-8.0	mV/°C	
Supply Current	I_S	-	4.0	7.0	µA	
Output Voltage	V_{OUT}	1.288	1.300	1.312	V	Ta = 30°C
Output Voltage Line Regulation	ΔV_{OUTVDD}	-	-	4	mV	V_{DD} = 2.4V to 5.5V
Output Voltage Load Regulation	ΔV_{OUTRL}	-	-	1	mV	Difference of I_{OUT}: 0µA/0.7µA

Typical Performance Curves

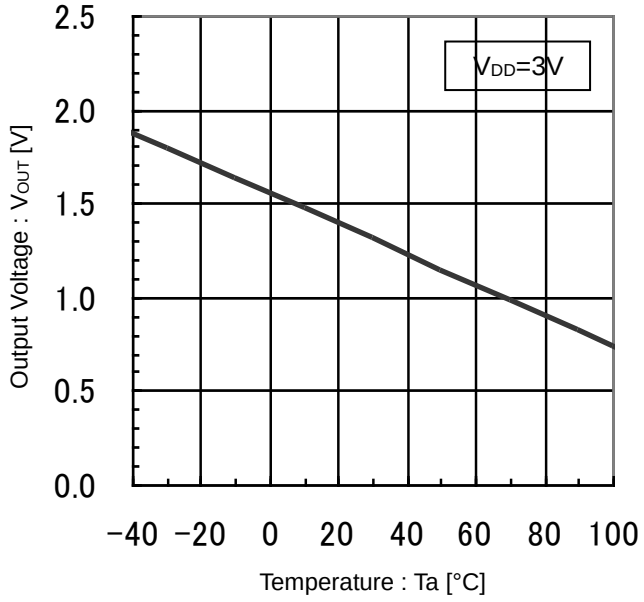


Figure 1. Output Voltage vs Temperature

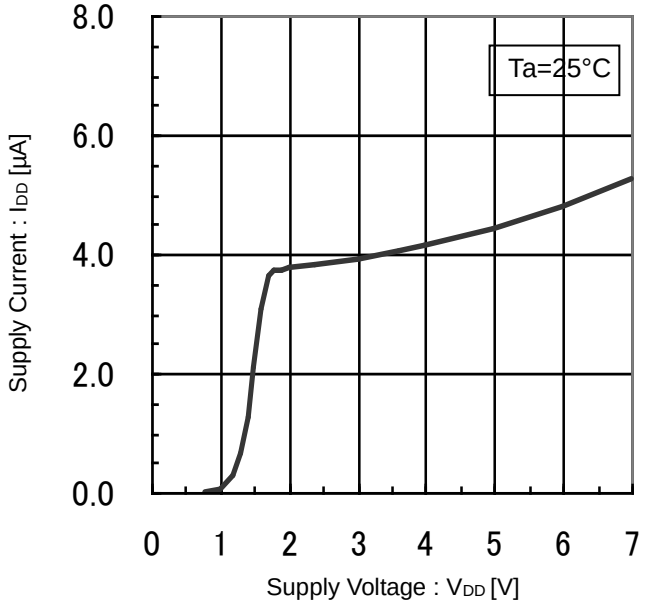


Figure 2. Supply Current vs Supply Voltage

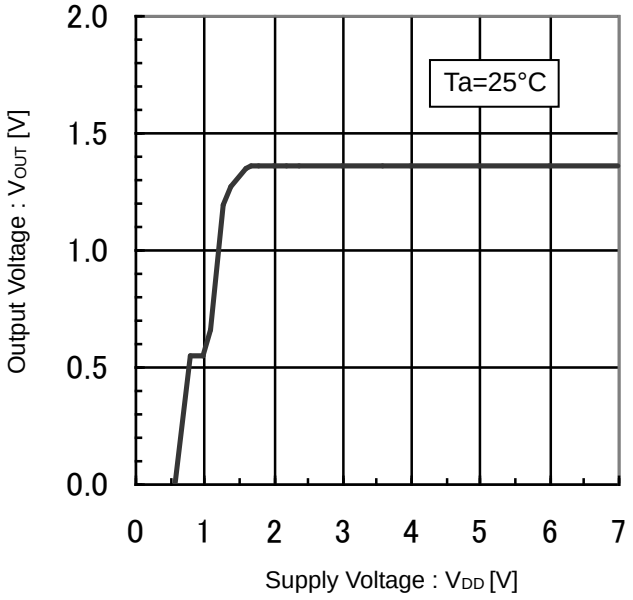


Figure 3. Output Voltage vs Supply Voltage

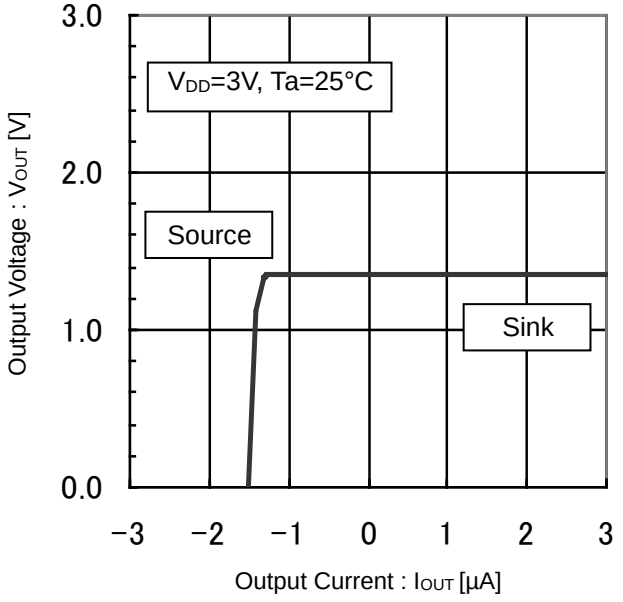


Figure 4. Output Voltage vs Output Current

Typical Performance Curves – continued

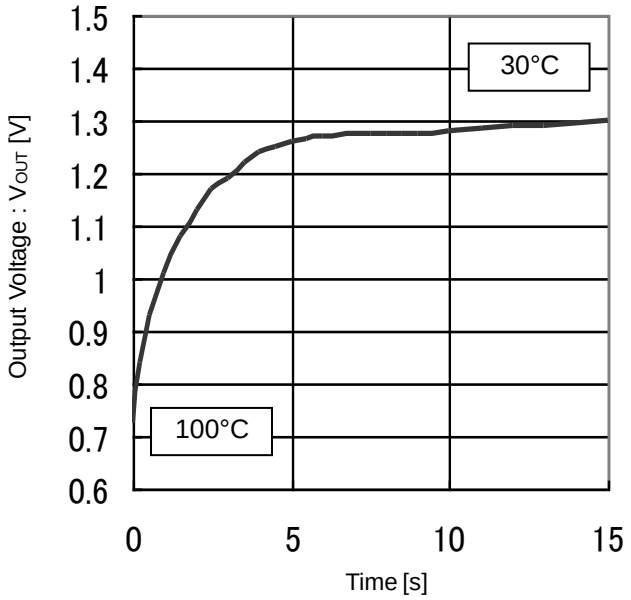
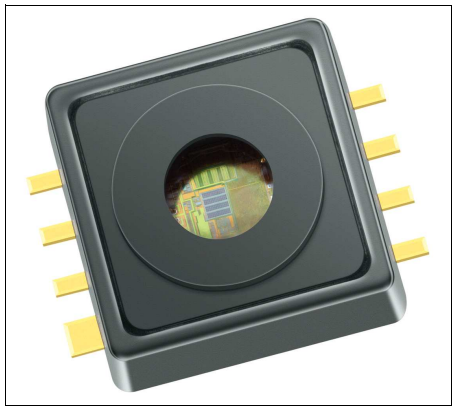


Figure 5. Start-up Response
(V_{OUT} response 100°C ~ 30°C in Atmosphere)

KP235

1 Product Description



The KP235 is a miniaturized Analog Barometric Air Pressure Sensor IC based on a capacitive principle. It is surface micromachined with a monolithic integrated signal conditioning circuit implemented in BiCMOS technology.
The sensor converts a pressure into an analog output signal. The calibrated transfer function converts a pressure of 40 kPa to 115 kPa into a voltage range of 0.5 V to 4.5 V.
The chip is packaged in a “green” SMD housing. The sensor has been primarily developed for measuring barometric air pressure, but can also be used in other application fields. The high accuracy and the high sensitivity of the device makes it a perfect fit for advanced automotive applications as well as in industrial and consumer applications.

1.1 Features

Following features are supported by the KP235:

- High precision pressure sensing (± 1.2 kPa)
- Ratiometric analog output
- Large temperature range (-40 ℃ to 125 ℃)
- Broken wire detection
- “Green” 8 pin SMD housing
- Automotive qualified

1.2 Target Applications

The KP235 is defined for use in following target applications:

- Automotive applications (barometric air pressure measurement)
- Industrial control
- Consumer applications
- Medical applications
- Weather stations
- Altimeters

Product Name	Product Type	Ordering Code	Package
Analog Absolute Pressure Sensor	KP235	SP000700776	PG-DSOF-8-16

2 Functional Description

The pressure is detected by an array of capacitive surface micromachined sensor cells. The sensor cell output is amplified, temperature compensated and linearized to obtain an output voltage that is proportional to the applied pressure.

The transfer function for linearization is computed in the digital part of the sensor using a third order polynomial calculation. The transfer function is created from the following parameters:

- Minimum and maximum rated pressure
- Voltage level at minimum and maximum rated pressure

The output is analog and ratiometric with respect to the supply voltage.

All parameters needed for the complete calibration algorithm — such as offset, gain, temperature coefficients of offset and gain, and linearization parameters — are determined after assembly. The parameters are stored in an integrated E^2PROM. The E^2PROM content is protected with forward error correction (a one bit error is detected and corrected, errors of more than one bit are detected and the output signal is switched to ground potential).

Open Bond Detection

When the chip is not powered properly, the JFET transistors of the broken wire detection stage are self-conducting. For example, if the GND connection is interrupted, the output is drawn strongly to VDD. Similarly, if the VDD connection is broken, the output is drawn to GND.

2.4 Transfer Function

The KP235 device is fully calibrated on delivery. The sensor has a linear transfer function between the applied pressure and the output signal:

$$V_{OUT} = V_{DD} \times (a \times P + b)$$

The output signal is ratiometric. Gain **a** and offset **b** are determined during calibration in order to generate the required transfer function.

Calibrated Transfer Function

The following calibration is adjusted with the parameters **a** and **b:**

Table 2 Transfer function

Pressure			Output Voltage @ $V_{DD} = V_{DD,Typ}$				Gain and Offset		
Symbol	**Values**	**Unit**	**Symbol**	**Values**	**Unit**		**Symbol**	**Value**	**Unit**
$p_{IN,1}$	40	kPa	$V_{OUT,1}$	0.5	V		*a*	0.01067	1/kPa
$p_{IN,2}$	115	kPa	$V_{OUT,2}$	4.5	V		*b*	-0.32667	–

Note: The points $p_{IN,1}/V_{OUT,1}$ and $p_{IN,2}/V_{OUT,2}$ define the calibrated transfer function and not the operating range. The operating pressure range is defined by the parameter 2.4 ***"Ambient operating pressure range" on Page 19***

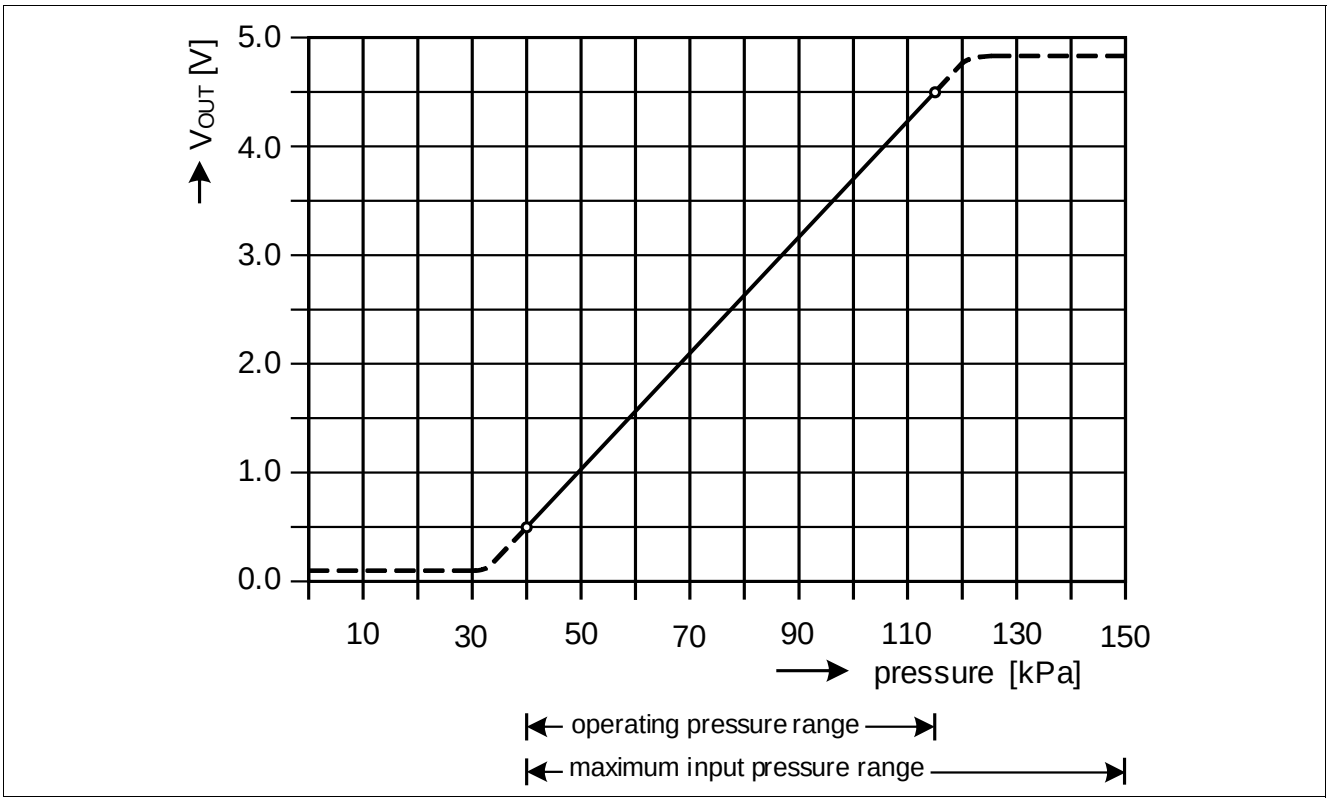


Figure 3 Transfer function

Note: The application circuitry determines the current driven by the device and thus may have an impact on the output voltage delivered by the sensor.

Note: Ratiometric signal error is not included in the overall accuracy. For error measurements, the supply voltage must have the nominal value ($V_{DD} = V_{DD,Typ}$).

The error band is determined by three continuous lines through four relevant breakpoints.

Table 4 Accuracy

Temperature [°C]	Error [kPa]	Error Multiplier
-40	±2.4	2.0
0	±1.2	1.0
85	±1.2	1.0
125	±2.4	2.0

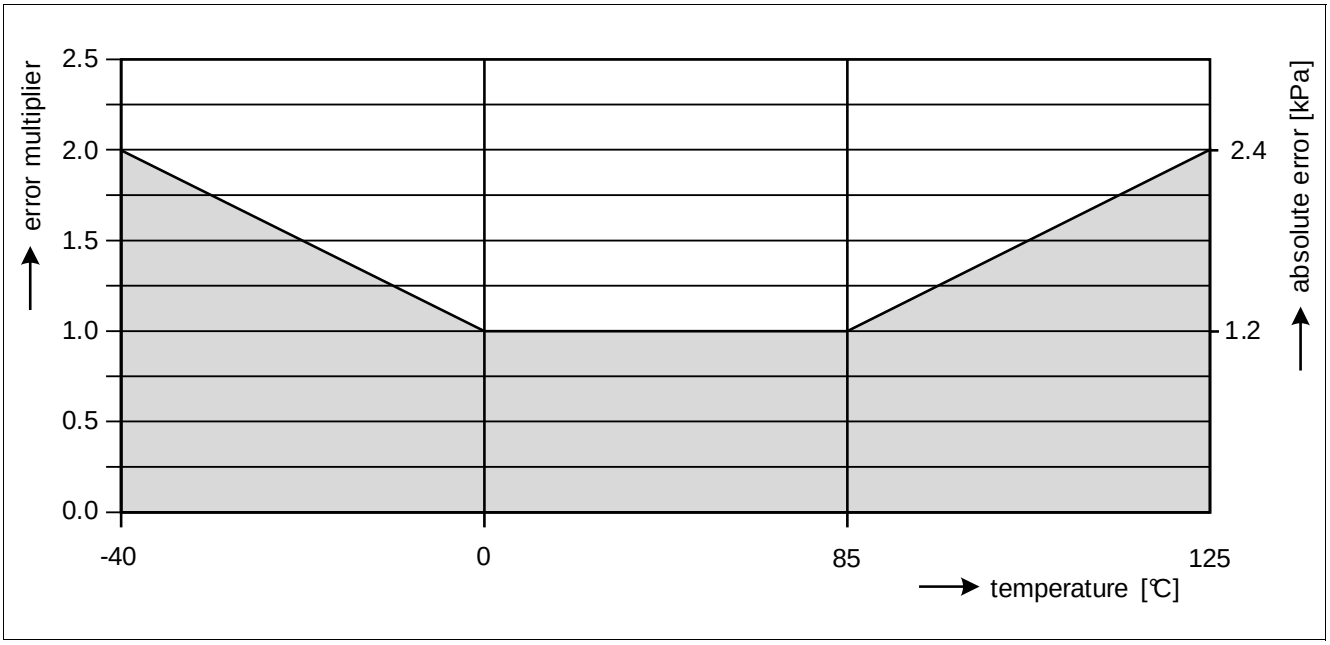


Figure 5 Accuracy for pressure acquisition

2.6 Output Voltage versus Load

The output voltage limits depend on:

- The value of the external load resistor.
- The type of connection (pull-up or pull-down).

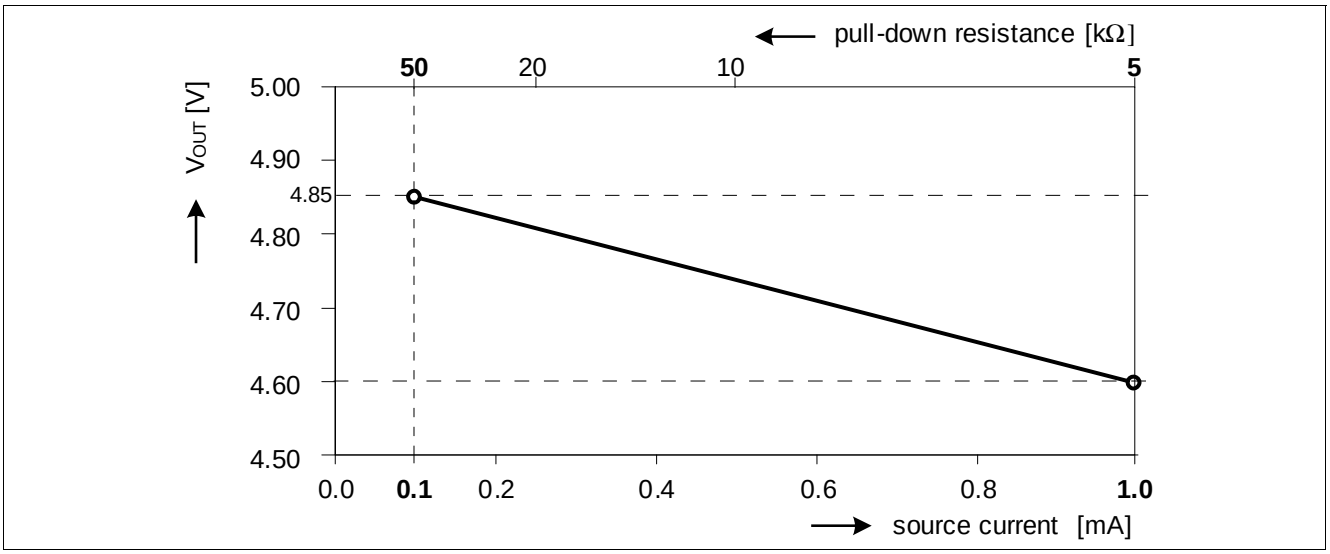


Figure 6 Maximum output voltage limit with pull-down load

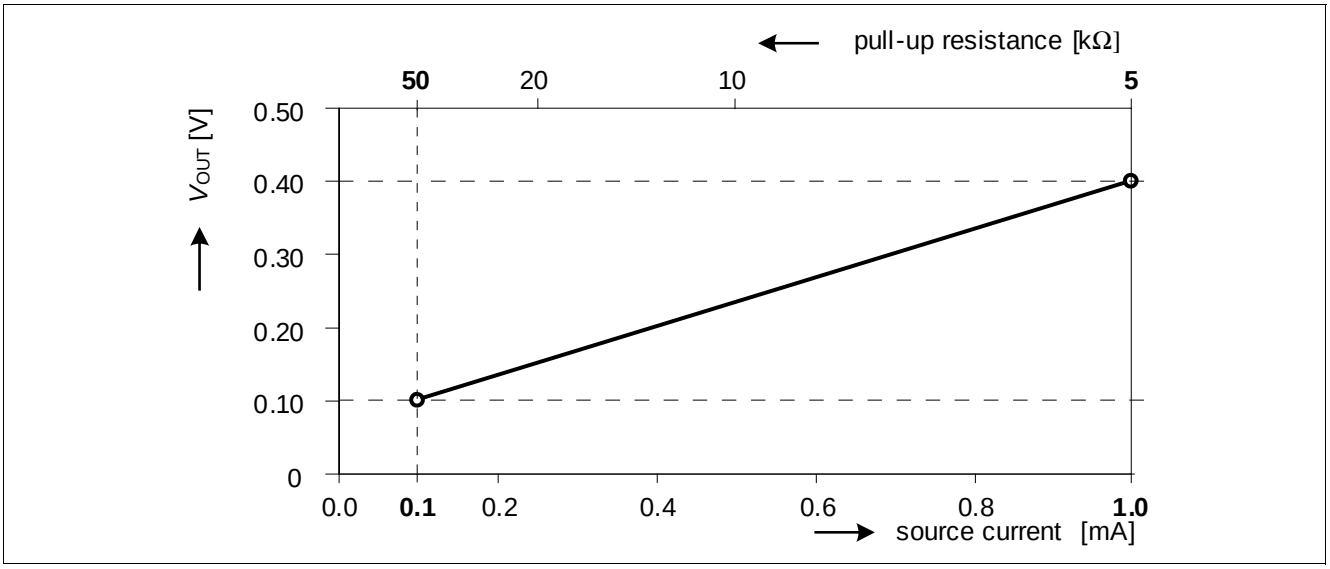


Figure 7 Minimum output voltage limit with pull-up load

Note: The values in the diagrams are valid for the entire specified temperature range.
The two diagrams above do not take into account clamping levels. In case clamping levels are implemented, the output voltage is clamped accordingly.

2.7 Timing Properties

Power-up Time

The power-up time t_{UP} is defined as the maximum time between the supply voltage reaching its operating range and the output voltage reaching 90% of its final value (assuming pin V_{OUT} open and constant input pressure).

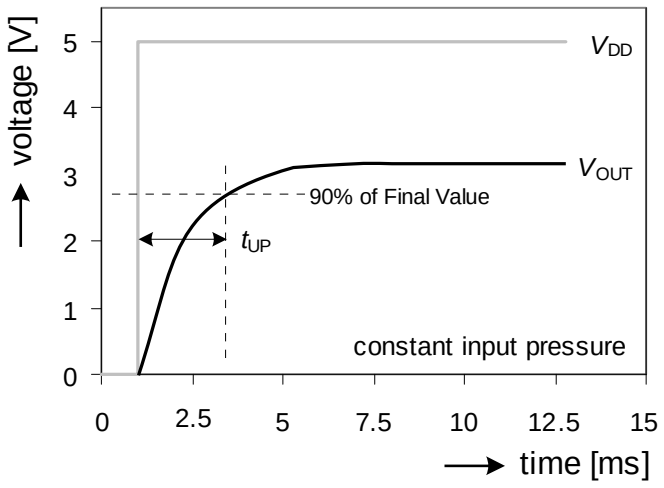


Figure 8 Power-up time

Response Time and Stabilization Time

The response time t_R is defined as the time required by the output to change from 10% to 90% of its final value after a specified pressure step (assuming pin V_{OUT} open).

The stabilization time t_S is defined as the time required by the output to meet the specified accuracy after the pressure has been stabilized (assuming pin V_{OUT} open).

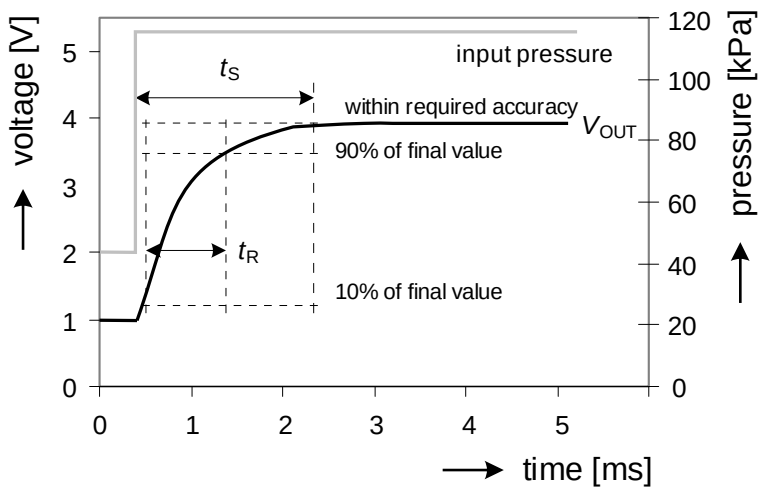


Figure 9 Response and stabilization time

Note: The values in the diagrams are valid for the entire specified temperature range.

3 Specification

3.1 Application Circuit Example

It is recommended to protect the pressure sensor IC against overload and electro-magnetic interferences (as shown in **Figure 10**).

The output circuit acts as a low-pass decoupling filter between the sensor IC output and the A/D input of the microcontroller.

The shown application circuit example considers an increased cable length between the sensor and the microcontroller. A combined location on a PCB with reduced distance between the sensor and the controller allows a reduction of the numbers of the passive components (e.g. C_2, R_1 and R_2 can be omitted).

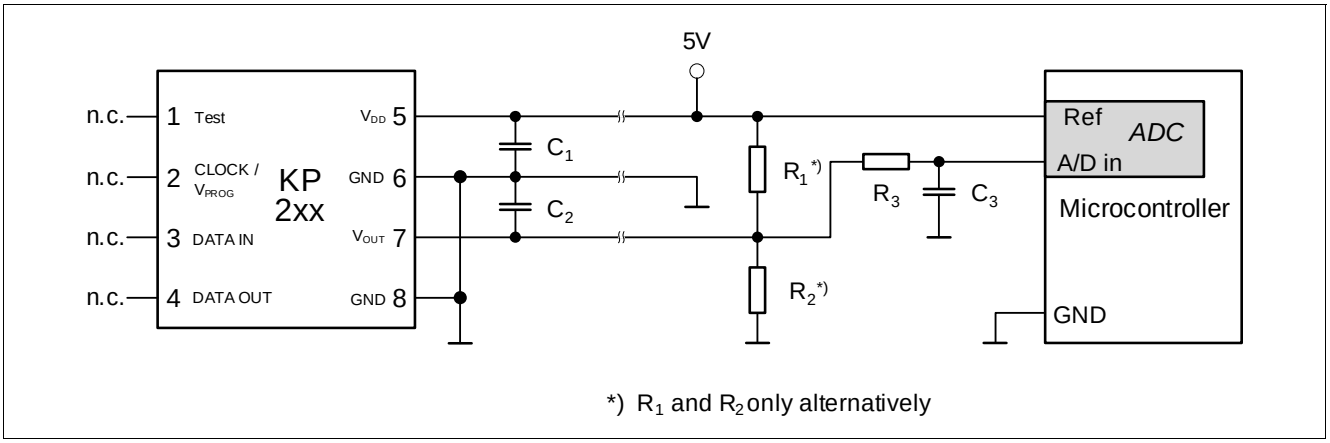


Figure 10 Application circuit example

Note: It is recommended to leave the digital pins CLOCK/V_{PROG}, DATA IN and DATA OUT floating (in case of an open GND connection, the floating pins prevent from a cross grounding through the corresponding ESD diodes).

Table 5 Component Values

Component	Symbol	Values			Unit
		Min.	Typ.	Max.	
Pull-Up Resistor	R_1	5	59	100	kΩ
Pull-Down Resistor	R_2	5	59	100	kΩ
Low Pass Resistor	R_3	3.9	22	100	kΩ
Supply Blocking Capacitor	C_1	10	100	100	nF
Output Blocking Capacitor	C_2	0	100	100	nF
Low Pass Capacitor	C_3	10	100	100	nF

3.2 Absolute Maximum Ratings

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage	V_{DD_max}	-0.3 – -6.5[1)]	– – –	6.5 16.5 –	V V V	– 1 h @ 70℃ Limited time: Max. 300 s	1.1
Output voltage	V_{OUT}	-0.3	–	V_{DD} + 0.3	V	–	1.2
Voltage on CLOCK / V_{PROG} pin	V_{CLK}	–	–	20	V	–	1.3
Voltage on DATA IN & DATA_OUT pins	V_{DATA}	–	–	5	V	–	1.4
Storage temperature	T_S	-60	–	150	℃	–	1.5
Thermal resistance	R_{thJA}	–	–	180	K/W	Thermal resistance between the die and ambient; according to JESD51-2	1.6
Maximum input pressure	p_{amb_max}	40	–	150 600	kPa kPa	 Limited time: Max. 300 s	1.7
ESD robustness (HBM: 1.5 kΩ, 100 pF)	V_{ESD}	–	–	2	kV	According to EIA / JESD22-A114-E	1.8

1) Reverse polarity; I_{DD} < 300 mA

Attention: Stresses above the max. values listed in Table 6 may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.3 Operating Range

The following operating conditions must not be exceeded in order to ensure correct operation of the device. All parameters specified in the following sections refer to these operating conditions, unless noted otherwise.

Table 7 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage	V_{DD}	4.5	5.0	5.5	V	V_{OUT} is ratiometric to V_{DD}	2.1
Output current on V_{OUT} pin	I_{OUT}	– -1	– –	1 –	mA mA	pull-down resistor used pull-up resistor used	2.2
Operating temperature	T_a	-40	–	125	°C		2.3
Ambient operating pressure range	p_{amb}	40	–	115	kPa		2.4
Lifetime[1)]	t_{live}	15	–	–	years		2.5

1) The life time shall be considered as anticipation with regard to the product that shall not extend the agreed warranty period.

3.4 Characteristics

Table 8 Electrical Characteristics

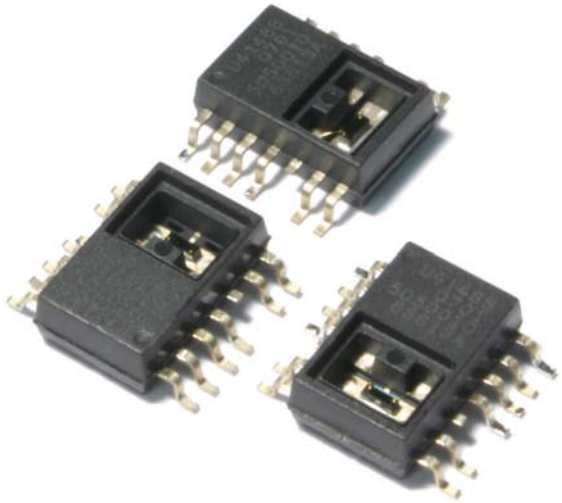
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output voltage range	V_{OUT_R}	0.10	–	4.85	V	See also section **"Output Voltage versus Load" on Page 15**	3.1
Supply current	I_{DD}	–	8	10	mA	During power up a peak supply current of max. 22 mA is possible	3.2
Output referred noise	V_{NOISE}	– –	– –	2.5 1.8	mV_{RMS} mV_{RMS}	Frequency > 1 kHz[1)] Frequency < 1 kHz	3.3
Response time[2)]	t_R	–	0.65	1.0[3)]	ms	10% to 90% of the final output value	3.4
Stabilization time[2)]	t_S	–	–	10	ms	For full accuracy	3.5
Power-up time[2)]	t_{UP}	–	–	5	ms	90% of the final output value	3.6
Broken wire: Diagnosis response time[4)]	t_{OBD}	–	–	1	ms		3.7
OBD transistor on resistance	R_{DSON}	–	–	160	Ω		3.8

1) 200 measurements in sequence, bandwidth limited to 40kHz
2) More details in section **"Timing Properties" on Page 16**
3) The maximum response time considers a maximal value of 100nF for the output blocking capacitor C_2 and a maximum pressure pulse equivalent 4.0V output change
4) In the event of a broken wire (broken VDD line or broken GND line), the output changes to certain voltage levels within the broken wire response time. The OBD ranges are determined by the application circuitry

GE
Sensing & Inspection Technologies

ChipCap

The Fully Calibrated Humidity and Temperature Solution



Features

- Simultaneous relative humidity and temperature outputs
- Precision accuracy ±2% RH, ±0.6°C
- Resolution 0.4% RH
- Factory selectable analog or digital outputs
- Output configurations available:
  Voltage 0V to 1V
  10 to 90% of VDD
  ZACwire™ digital output (8-bit humidity)
- Factory calibrated, ready to use
- Designed for automated assembly
- Supply voltage: 3.0V to 5.5V
- Low quiescent current: 0.5mA@5V, 25°C
- SOP 14 package

Applications

- HVAC Controls
  — Humidistats
  — Enthalpy control
  — Indoor air quality (IAQ)
  — Humidifiers
  — Dehumidifiers
- Instrumentation
  — Portable instruments
  — Data loggers and recorders
  — Weather stations
- Medical
  — Nebulizers
  — Oxygen air
  — CPAP/Sleep apnea devices
- Automotive
  — Cabin climate control
  — Defrost control
- Appliances and white goods
- OEM assemblies available

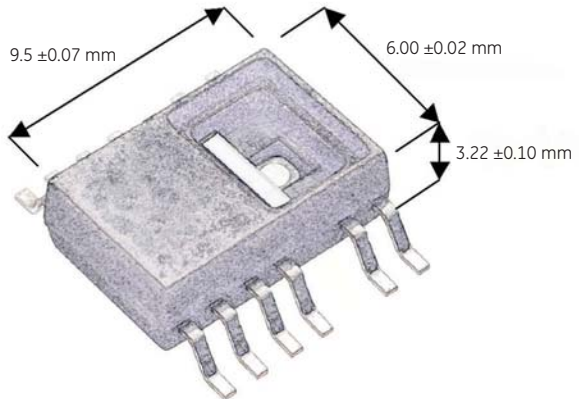
ChipCap—The Fully Calibrated Humidity and Temperature Sensor

The ChipCap series humidity sensor by GE offers a new standard in the field of accurate relative humidity measurement. Based on a capacitive polymer sensing technology, this device offers signal conditioning and temperature compensation for a single SoC (Systemon-Chip) solution. The device is very simple to use, fully tested and calibrated for accuracy on delivery—no further calibration is needed. ChipCap can be incorporated into an assembly or finished sensor to meet customer specifications. The measurement is accurate to ±2% from 20% to 80% RH and ±3% across the entire humidity range. Long term stability is excellent. The temperature accuracy is ±1°C from 0°C to +70°C. Dual outputs provide humidity and temperature as 0V to 1V, or 0.5V to 4.5V ratiometric or available with digital output (the ZACwire one-wire interface).

Accurate, Repeatable Humidity and Temperature Measurement

ChipCap provides either analog or digital interfaces on a single, 5VDC-powered chip. The package is highly resistant to chemical vapors and other contaminants. ChipCap sensors are precalibrated and offer high interchangeability. They also fully recover from condensing environments and may be used across a wide range of both temperature and relative humidity ranges.

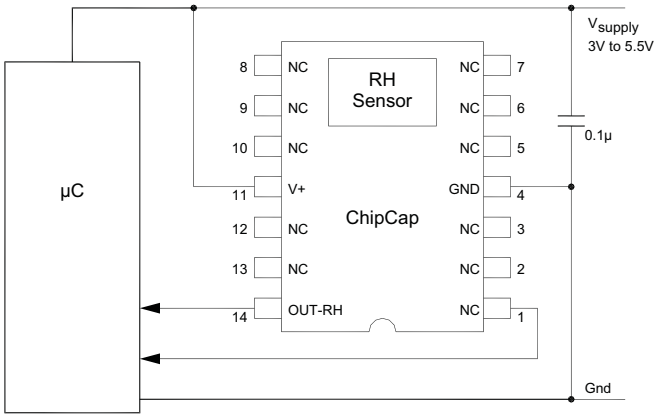
ChipCap relative humidity sensors change capacitance in direct proportion to ambient relative humidity. An internal solid-state band gap provides temperature measurement. This integral design reduces overall cost and complexity and improves reliability.



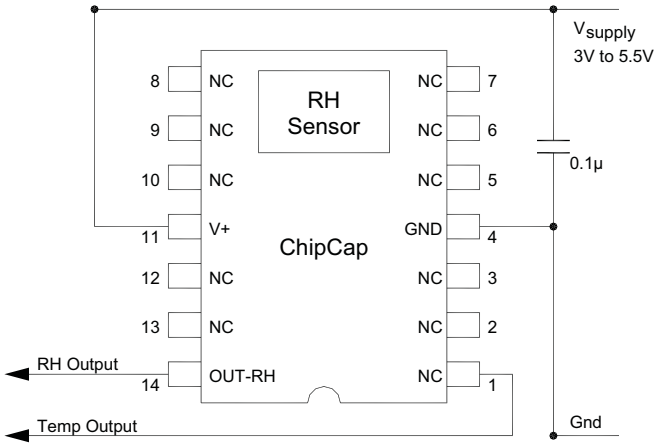
Small, Integrated Package for Automated Assembly

ChipCap contains the entire signal conditioning circuitry on a single silicon die. The sensor and circuitry are integrated into a small footprint SoC to save board real estate. ChipCap is shipped in tube packaging for automated insertion on surface mount technology (SMT) circuit boards. Tape and reel packaging is available upon request for high volume applications.

Digital Interface



Analog Interface



Linear mode:

%RH = Vout * 100
Tc = Vout * 200 -50

Ratiometric mode:

%RH = ((Vout - (0.1 * Vsupply))/(0.8 * Vsupply)) * 100
Tc = ((Vout - (0.1 * Vsupply))/(0.8 * Vsupply)) * 200 - 50

ChipCap Specifications

Relative Humidity

RH Sensor
Planar Capacitive Polymer

RH Range
0 to 100% RH

RH Accuracy @ 25°C
±2% from 20% to 80%
±3% from 0% to 20% and 80% to 100%

RH Resolution
0.4% RH

Temperature

Temperature Sensor
Integral band gap PTAT

Temperature Scale
-50°C to 150°C

Temperature Accuracy
±0.6°C at 25°C (see graph below)

Temperature Resolution
0.2°C

Power Supply

Reverse Polarity Protection
12.5 VDC, 100µA (15VDC, 60s)

Voltage Supply
3 to 5.5 VDC

Current Supply
500 microamps @ 5 VDC, 25°C

Outputs

RH Voltage Output (Ratiometric)
Vout = (Vsupply/5)(0.5+(.04*RH)); 0.5 to 4.5V ratiometric; 5VDC nom.

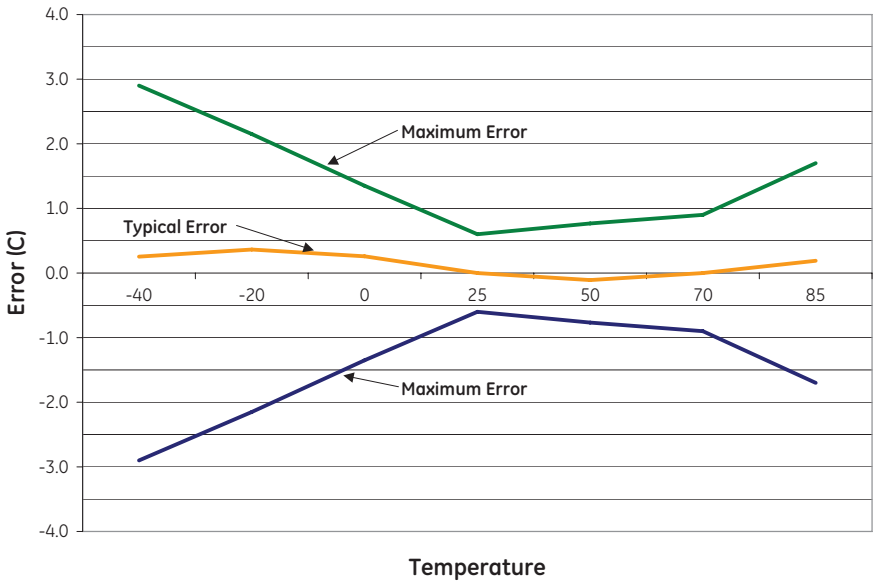
RH Voltage Output (Linear, 0-1V)
Vout = 0.01(RH)

RH Digital Output
Manchester 8-bit encoded

Temperature Voltage Output (Ratiometric)
Vout = (Vsupply/5)(1.5 + (.02*T°C)); 0.5 to 4.5V ratiometric; 5VDC nom.

Temperature Voltage Output (Linear)
Vout = (0.005T °C) +0.25

Temperature Digital Output
Manchester 10-bit encoded



Environmental

Operating Temperature Range
-40°C to 85°C

Operating RH Range
0 to 100 % RH, non-condensing

Packaging

Packaging
SOP-14, SMD

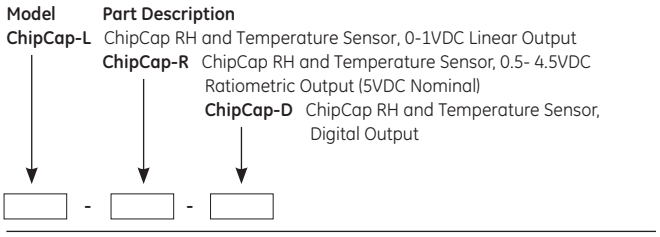
Soldering
IR Solder Reflow, 260°C, 10 sec

Pin Connection
4 Pin; +V, Gnd, RHout, Tout

Absolute Maximum Ratings					
Symbol	Parameter	Min.	Max.	Units	Notes
Vdd	DC Supply Voltage	-0.3	6	V	
Vio	Voltage at all Analog and Digital I/O pins	-0.3	Vdd + 0.3	V	
Ta	Ambient Temperature (operation)	-50 -40	150 85	°C °C	ASIC RH Sensor
Tstrg	Storage Temperature	-55	150	°C	
Tj	Junction Temperature	-55	160	°C	

Recommended Operation Conditions						
Symbol	Parameter	Min.	Type	Max.	Units	Notes
Vdd	Analog DC Supply	3	5	5.5	V	
Idd	Supply Current		550		µA	25°C
Vss	Analog Ground		0.0		V	
To	Ambient Temperature	-40	27	85	°C	
Cvdd	External Capacitance between Vdd and Vss	100	220	470	nF	
C_{LD}	Digital Output Load (only capacitive, no resistive)			100	pF	
C_{LA}	Analog Output Load Capaictance			5	nF	
R_{LA}	Analog Output Load Resistance	5			KΩ	

Ordering Information



www.gesensinginspection.com

920-426B

Low-Noise, 900kHz, RRIO, Precision OPERATIONAL AMPLIFIER Zerø-Drift Series

Check for Samples: OPA378 OPA2378

FEATURES

- **LOW NOISE**
  - **0.4μV$_{PP}$, 0.1Hz to 10Hz**
  - **20nV/√Hz at 1kHz**
- **ZERØ-DRIFT SERIES**
  - **LOW OFFSET VOLTAGE: 20μV**
  - **LOW OFFSET DRIFT: 0.1μV/°C**
- **QUIESCENT CURRENT: 125μA**
- **GAIN BANDWIDTH: 900kHz**
- **RAIL-TO-RAIL INPUT/OUTPUT**
- **EMI FILTERING**
- **SUPPLY VOLTAGE: 2.2V to 5.5V**
- ***micro*SIZE PACKAGES: SC70 and SOT23**

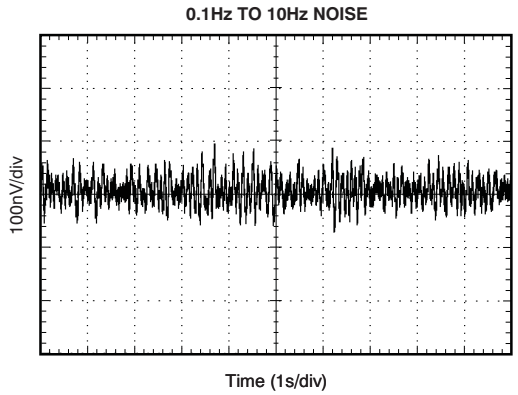
APPLICATIONS

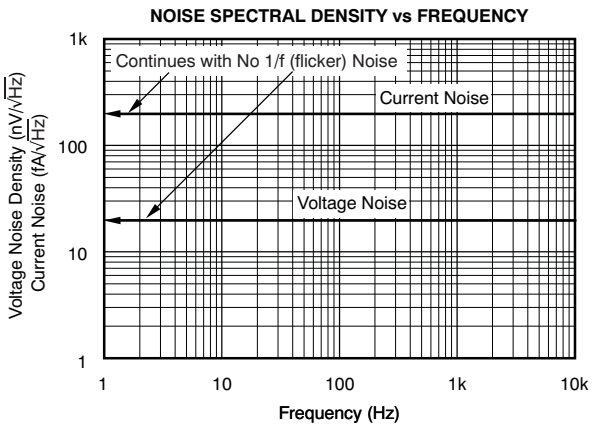
- **PORTABLE MEDICAL DEVICES**
  - **GLUCOSE METERS**
  - **OXYGEN METERING**
  - **HEART RATE MONITORS**
- **WEIGH SCALES**
- **BATTERY-POWERED INSTRUMENTS**
- **THERMOPILE MODULES**
- **HANDHELD TEST EQUIPMENT**
- **SENSOR SIGNAL CONDITIONING**

DESCRIPTION

The OPA378 and OPA2378 represent a new generation of Zerø-Drift, microPOWER™ operational amplifiers that use a proprietary auto-calibration technique to provide minimal input offset voltage (20μV) and offset voltage drift (0.1μV/°C). The combination of low input voltage noise, high gain bandwidth (900kHz), and low power (150μA max) enable these devices to achieve optimum performance for low-power precision applications. In addition, the excellent PSRR performance, coupled with a wide input supply range of 2.2V to 5.5V and rail-to-rail input and output, makes it an outstanding choice for single-supply applications that run directly from batteries without regulation.

The OPA378 (single version) is available in both a *micro*SIZE SC70-5 and a SOT23-5 package. The OPA2378 (dual version) is offered in a SOT23-8 package. All versions are specified for operation from –40°C to +125°C.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA378	SOT23-5	DBV	OAZI
OPA378	SC70-5	DCK	BTS
OPA2378	SOT23-8	DCN	OCAI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

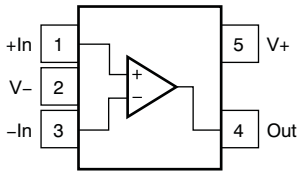
Over operating free-air temperature range (unless otherwise noted).

		OPA378, OPA2378	UNIT
Supply Voltage, V_S = (V+) – (V–)		+7	V
Signal Input Terminals	Voltage(2)	(V–) – 0.3 ≤ V_{IN} ≤ (V+) + 0.3	V
	Current(2)	±10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature, T_A		–55 to +150	°C
Storage Temperature, T_A		–65 to +150	°C
Junction Temperature, T_J		+150	°C
ESD Ratings	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

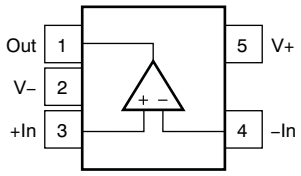
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

PIN CONFIGURATIONS

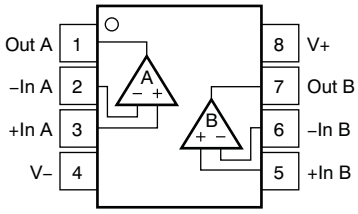
OPA378 SC70-5 (TOP VIEW)



OPA378 SOT23-5 (TOP VIEW)



OPA2378 SOT23-8 (TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA378, OPA2378 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage, OPA378	V_{OS}	V_{CM} = V–		20	50	µV
vs Temperature	**dV_{OS}/dT**			**0.1**	**0.25**	**µV/°C**
Input Offset Voltage, OPA2378				20	70	µV
vs Temperature	**dV_{OS}/dT**	**-40°C to +125°C**		**0.25**	**0.4**	**µV/°C**
		–40°C to +85°C		0.15	0.25	µV/°C
vs Power Supply, OPA378	PSRR	V_{CM} = 0V, V_S = +2.2V to +5.5V		1.5	5	µV/V
over Temperature		**V_{CM} = 0V, V_S = +2.2V to +5.5V**		**3**	**8**	**µV/V**
vs Power Supply, OPA2378		V_{CM} = 0V, V_S = +2.2V to +5.5V			10	µV/V
over Temperature		**V_{CM} = 0V, V_S = +2.2V to +5.5V**		**3**	**13**	**µV/V**
Channel Separation (Dual Version)		At dc		135		dB
INPUT BIAS CURRENT						
Input Bias Current, OPA378	I_B			±150	±550	pA
Input Bias Current, OPA2378				±150	±670	pA
over Temperature, OPA378 and OPA2378					**±2**	**nA**
Input Offset Current, OPA378	I_{OS}			±0.3	±1.1	nA
Input Offset Current, OPA2378				±0.3	±1.34	nA
NOISE						
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz, V_S = +5.5V		0.4		$µV_{PP}$
Input Voltage Noise Density	e_n	f = 1kHz		20		nV/√Hz
Input Current Noise	i_n	f = 10Hz		200		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.05		(V+) + 0.05	V
Common-Mode Rejection Ratio	CMRR	(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 5.5V	100	112		dB
		(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 2.2V	94	106		dB
over Temperature		**(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 5.5V**	**96**			**dB**
		(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 2.2V	**90**			**dB**
INPUT CAPACITANCE						
Differential	C_{IN}			4		pF
Common-Mode				5		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	50mV < V_O < (V+) – 50mV, R_L = 100kΩ	110	134		dB
		100mV < V_O < (V+) – 100mV, R_L = 10kΩ	110	130		dB
over Temperature		**100mV < V_O < (V+) – 100mV, R_L = 10kΩ**	**106**			**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			900		kHz
Slew Rate	SR	G = +1		0.4		V/µs
Settling Time 0.1%	t_S	V_S = 5.5V, 2V Step, G = +1		7		µs
Settling Time 0.01%	t_S	V_S = 5.5V, 2V Step, G = +1		9		µs
Overload Recovery Time		V_{IN} × Gain > V_S		4		µs
THD + Noise	THD + N	V_S = 5V, V_O = $3V_{PP}$, G = +1, f = 1kHz		0.003		%

ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA378, OPA2378 MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail, OPA378	V_O	R_L = 10kΩ		6	8	mV
over Temperature		**R_L = 10kΩ**		**8**	**13**	**mV**
Voltage Output Swing from Rail, OPA2378	V_O	R_L = 10kΩ		6	10	mV
over Temperature		**R_L = 10kΩ**		**8**	**15**	**mV**
Voltage Output Swing from Rail		R_L = 100kΩ		0.7	2	mV
over Temperature		**R_L = 100kΩ**			**3**	**mV**
Short-Circuit Current	I_{SC}			±30		mA
Capacitive Load Drive	C_{LOAD}			See Figure 18		pF
Open-Loop Output Impedance	Z_O			See Figure 23		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.2		5.5	V
Quiescent Current (per Amplifier)	I_Q	I_O = 0mA, V_S = +5.5V		125	150	µA
over Temperature					**165**	**µA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5				200		°C/W
SC70-5				250		°C/W
SOT23-8				100		°C/W

TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

0.1Hz TO 10Hz NOISE

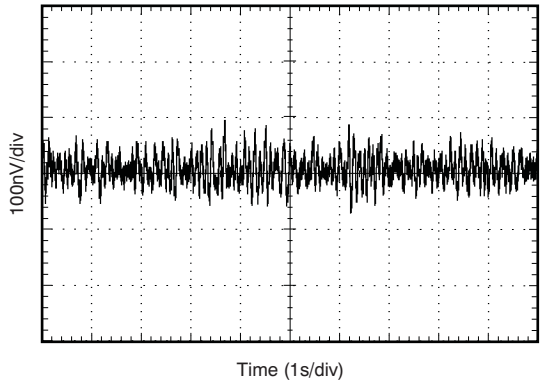


Figure 1.

INPUT CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

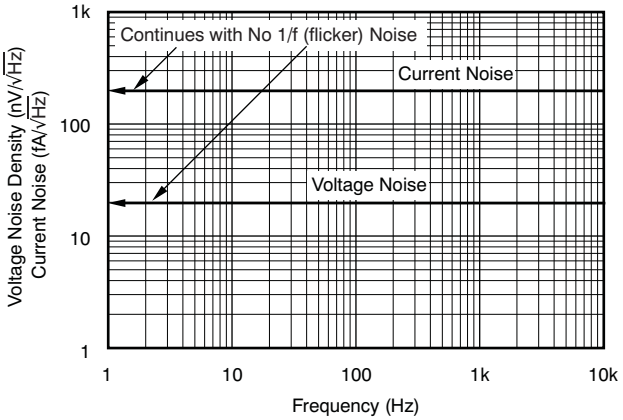


Figure 2.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

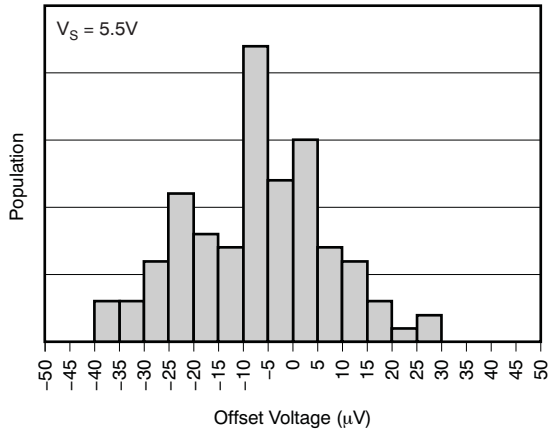


Figure 3.

OFFSET VOLTAGE DRIFT DISTRIBUTION

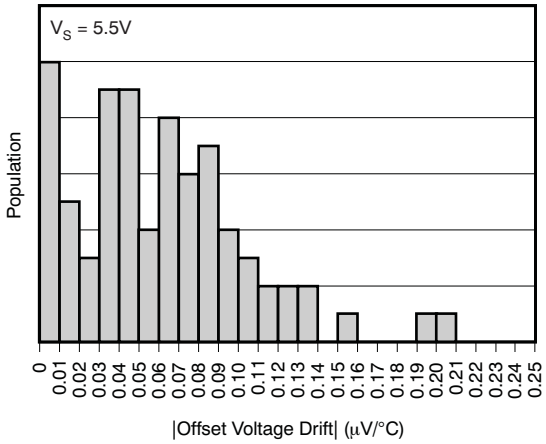


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

OFFSET VOLTAGE vs TEMPERATURE

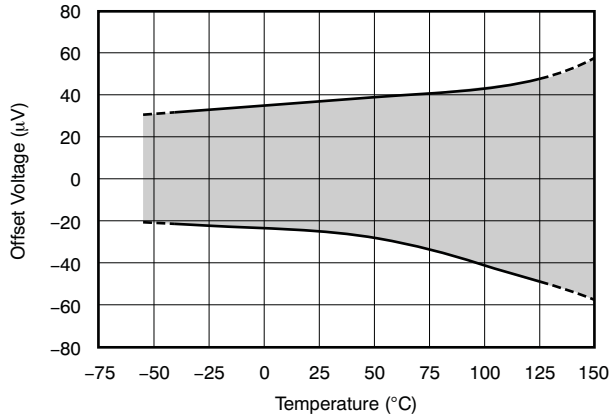


Figure 5.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

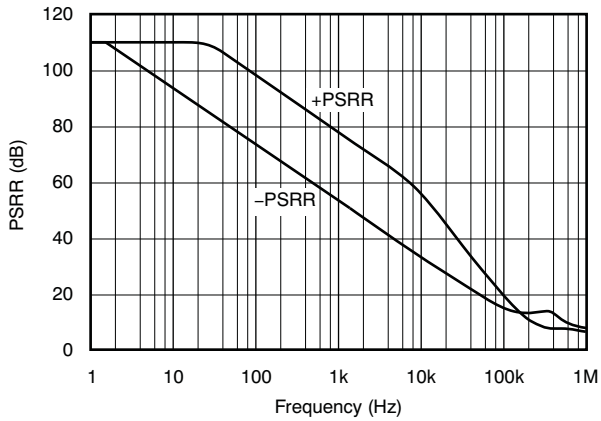


Figure 6.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

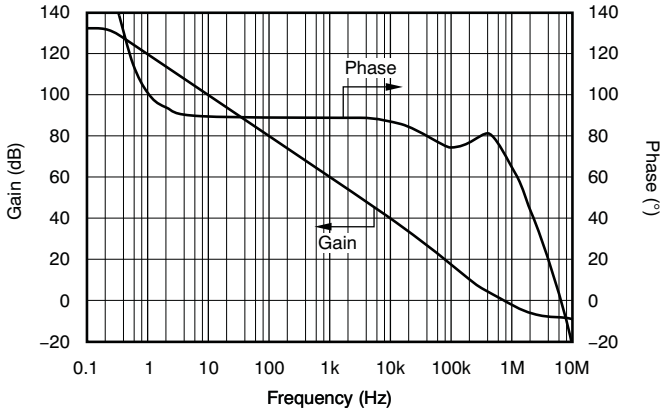


Figure 7.

OPEN-LOOP GAIN vs TEMPERATURE

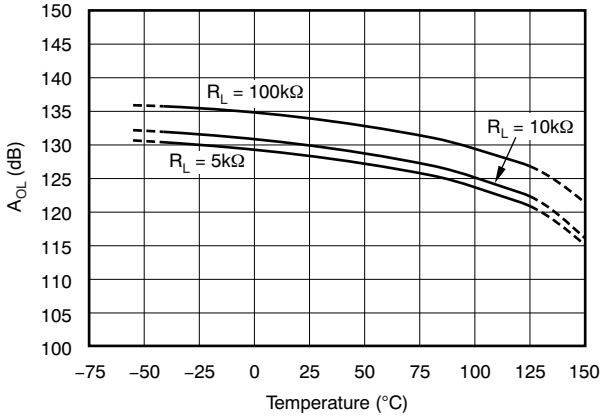


Figure 8.

COMMON-MODE REJECTION RATIO vs FREQUENCY

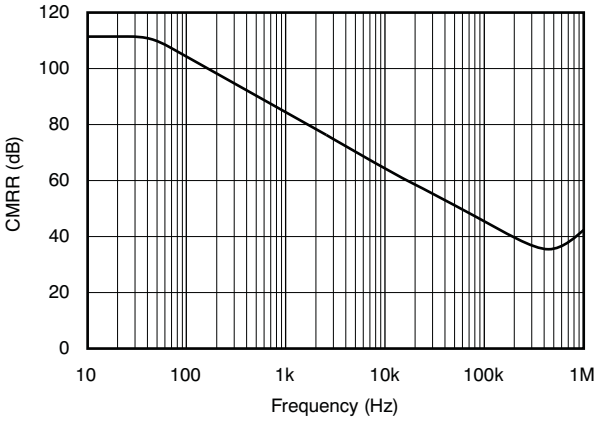


Figure 9.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE

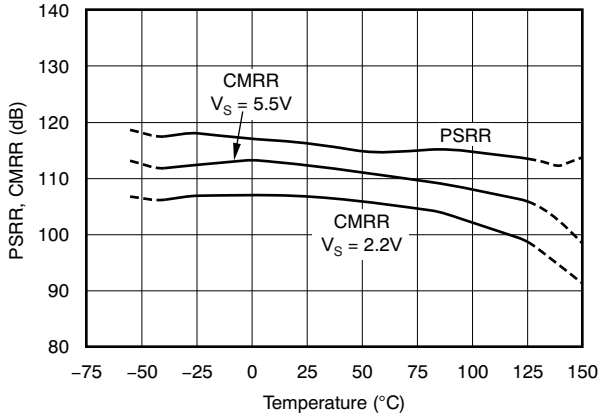
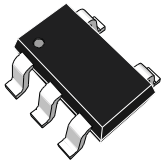


Figure 10.

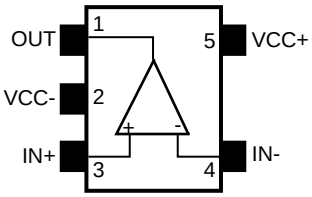
TSB611

Low-power, rail-to-rail output, 36 V operational amplifier

Datasheet - production data



SOT23-5



Features

- Low offset voltage: 1 mV max
- Low power consumption: 125 µA max. at 36 V
- Wide supply voltage: 2.7 to 36 V
- Gain bandwidth product: 560 kHz typ
- Unity gain stable
- Rail-to-rail output
- Input common mode voltage includes ground
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive qualification

Applications

- Industrial
- Power supplies
- Automotive

Description

The TSB611 single operational amplifier (op amp) offers an extended supply voltage operating range and rail-to-rail output. It also offers an excellent speed/power consumption ratio with 560 kHz gain bandwidth product while consuming less than 125 µA at 36V supply voltage.

The TSB611 operates over a wide temperature range from -40 °C to 125°C making this device ideal for industrial and automotive applications.

Thanks to its small package size, the TSB611 can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

1 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage [(1)]	40	V
V_{id}	Differential input voltage [(2)]	$\pm V_{cc}$	
V_{in}	Input voltage	(V_{cc-}) - 0.2 to (V_{cc+}) + 0.2	
I_{in}	Input current [(3)]	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient [(4)(5)]	250	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model [(6)]	4000	V
	MM: machine model [(7)]	200	
	CDM: charged device model [(8)]	1500	
	Latch-up immunity	200	mA

Notes:

(1)All voltage values, except differential voltage are with respect to network ground terminal.

(2)Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3)Input current must be limited by a resistor in series with the inputs.

(4)R_{th} are typical values.

(5)Short-circuits can cause excessive heating and destructive dissipation.

(6)According to JEDEC standard JESD22-A114F.

(7)According to JEDEC standard JESD22-A115A.

(8)According to ANSI/ESD STM5.3.1.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	2.7 to 36	V
V_{icm}	Common mode input voltage range	(V_{cc-}) - 0.1 to (V_{cc+}) - 1	
T_{oper}	Operating free air temperature range	-40 to 125	°C

2 Electrical characteristics

Table 3: Electrical characteristics at Vcc+ = 2.7 V with Vcc- = 0 V, Vicm = Vcc/2, Tamb = 25 °C, and RL = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-1		1	mV
		-40 °C < T< 125 °C	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C		1.8	6	µV/°C
I_{io}	Input offset current			1	5	nA
		-40 °C < T< 125 °C			10	
I_{ib}	Input bias current			5	10	
		-40 °C < T< 125 °C			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 V to V_{cc+} -1 V, V_{out} = V_{cc}/2	90	115		dB
		-40 °C < T< 125 °C	85			
A_{vd}	Large signal voltage gain	V_{out} = 0.5 V to (V_{cc+} - 0.5 V)	98	102		
		-40 °C < T< 125 °C	94			
V_{OH}	High level output voltage (voltage drop from V_{cc+})			13	25	mV
		-40 °C < T< 125 °C			30	
V_{OL}	Low level output voltage			26	30	
		-40 °C < T< 125 °C			35	
I_{out}	I_{sink}	V_{out} = V_{cc}	13	20		mA
		-40 °C < T< 125 °C	10			
	I_{source}	V_{out} = 0 V	20	28		
		-40 °C < T< 125 °C	7			
I_{CC}	Supply current (per channel)	No load, V_{out} = V_{cc}/2		92	110	µA
		-40 °C < T< 125 °C			125	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		480		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		430		
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		18		dB
SR+	Positive slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.13	0.18		V/µs
SR-	Negative slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.10	0.14		
e_n	Equivalent input noise voltage	f = 1 kHz		37		nV/√Hz
		f = 10 kHz		32		
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} - 1 V)/2, BW = 22 kHz, V_{out} = 1 V_{pp}		0.005		%

Table 4: Electrical characteristics at Vcc+ = 12 V with Vcc- = 0 V, Vicm = Vcc/2, Tamb = 25 °C, and RL = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-1		1	mV
		-40 °C < T< 125 °C	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C		1.6	6	µV/°C
I_{io}	Input offset current			1	5	nA
		-40 °C < T< 125 °C			15	
I_{ib}	Input bias current			5	10	
		-40 °C < T< 125 °C			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 V to V_{cc+} - 1 V, V_{out} = $V_{cc}/2$	95	126		dB
		-40 °C < T< 12 5°C	90			
SVR	Supply voltage rejection ratio: 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{cc} = 2.8 to 12 V	95	124		
		-40 °C < T< 125 °C	90			
A_{vd}	Large signal voltage gain	V_{out} = 0.5 V to (V_{cc+} - 0.5 V)	105	115		
		-40 °C < T< 125 °C	100			
V_{OH}	High level output voltage drop from V_{cc+}			37	60	mV
		-40 °C < T< 125 °C			65	
V_{OL}	Low level output voltage			56	65	
		-40 °C < T< 125 °C			75	
I_{out}	I_{sink}	V_{out} = V_{cc}	24	35		mA
		-40 °C < T< 125 °C	10			
	I_{source}	V_{out} = 0 V	28	40		
		-40 °C < T< 125 °C	10			
I_{CC}	Supply current (per channel)	No load, V_{out} = $V_{cc}/2$		97	115	µA
		-40 °C < T< 125 °C			130	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		510		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		460		
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		18		dB
SR+	Positive slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.13	0.19		V/µs
SR-	Negative slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.11	0.15		
e_n	Equivalent input noise voltage	f = 1 kHz		31		nV/√Hz
		f = 10 kHz		30		
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} - 1 V)/2, BW = 22 kHz, V_{out} = 2 V_{pp}		0.004		%

Figure 1: Supply current vs. supply voltage at Vicm = VCC/2

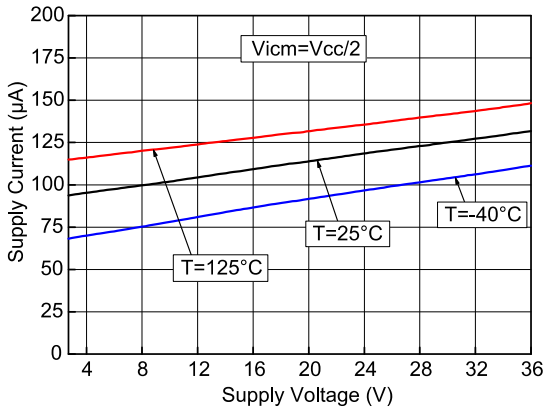


Figure 2: Input offset voltage distribution at VCC = 2.7 V

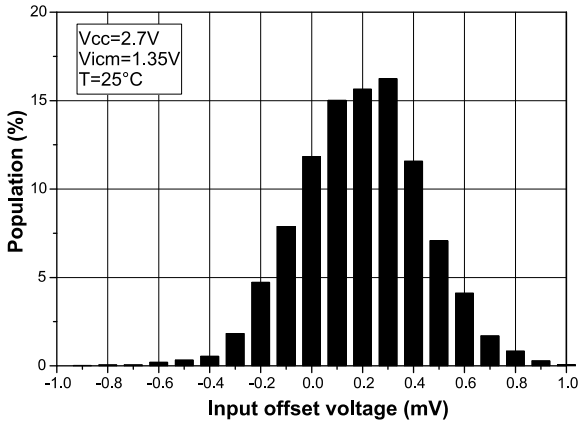


Figure 3: Input offset voltage distribution at VCC = 12 V

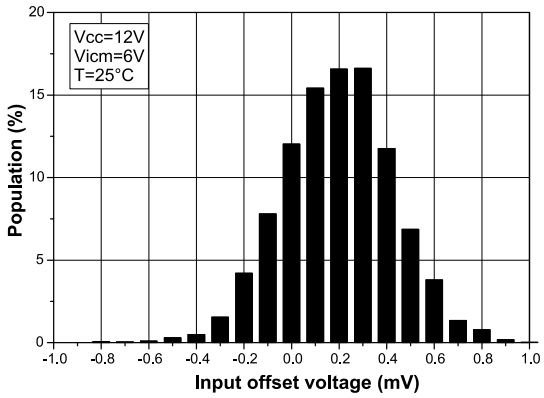


Figure 4: Input offset voltage distribution at VCC = 36 V

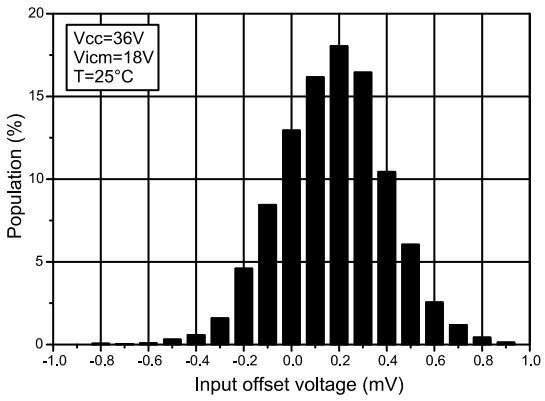


Figure 5: Input offset voltage vs. Temperature at VCC = 36 V

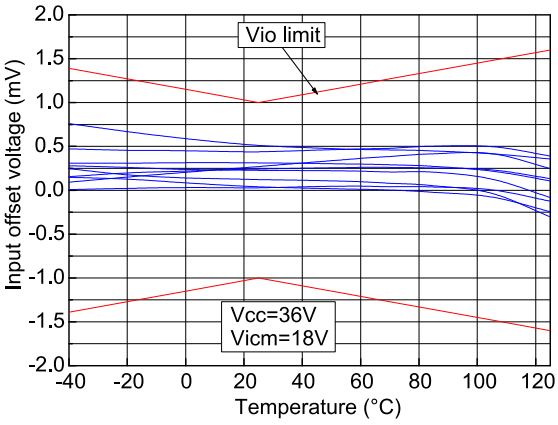


Figure 6: Input offset voltage temperature variation distribution at VCC = 36 V

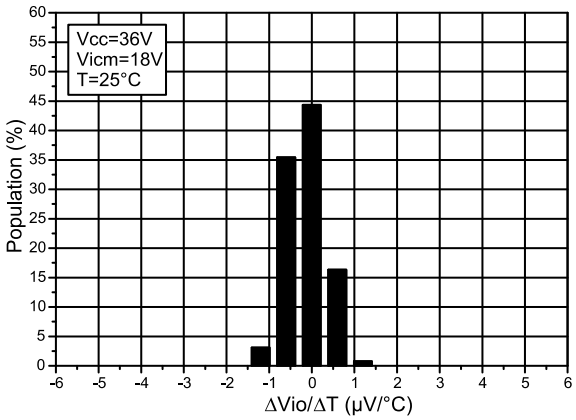


Figure 7: Input offset voltage vs. supply voltage

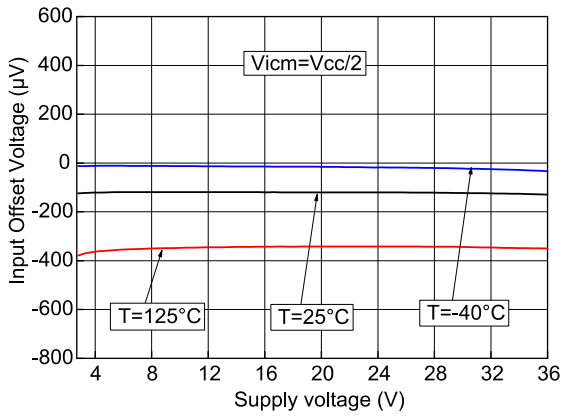


Figure 8: Input offset voltage vs. common-mode voltage at VCC = 2.7 V

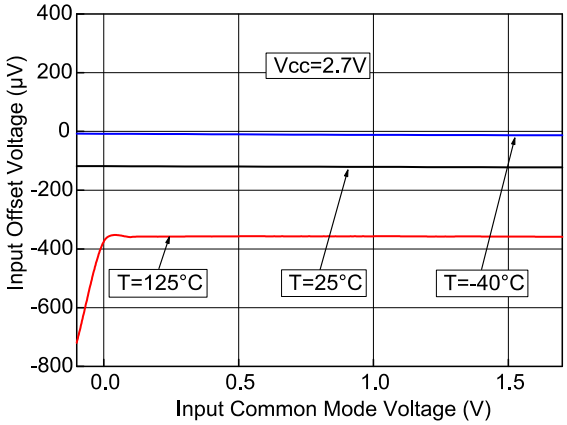


Figure 9: Input offset voltage vs. common-mode voltage at VCC = 36 V

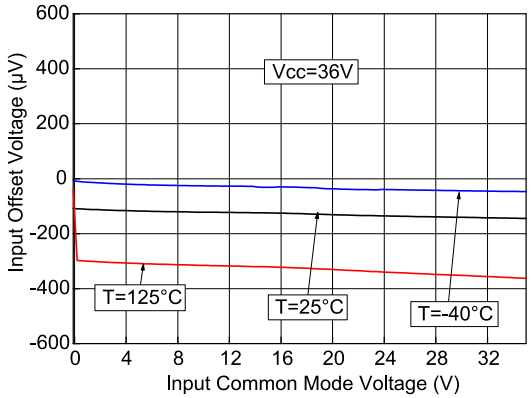


Figure 10: Input bias current vs. common mode voltage at VCC = 4 V

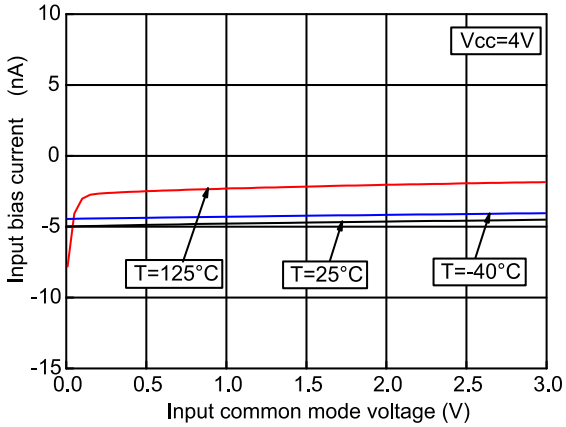


Figure 11: Input bias current vs. common mode voltage at VCC = 36 V

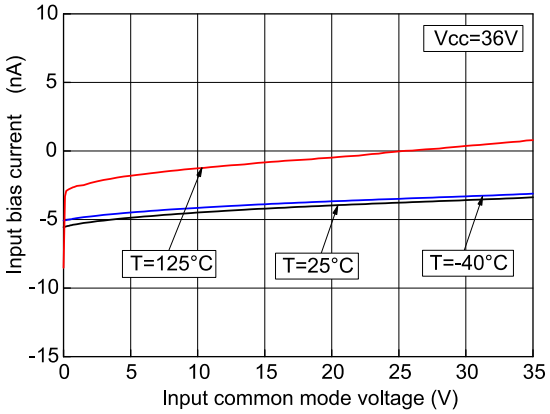
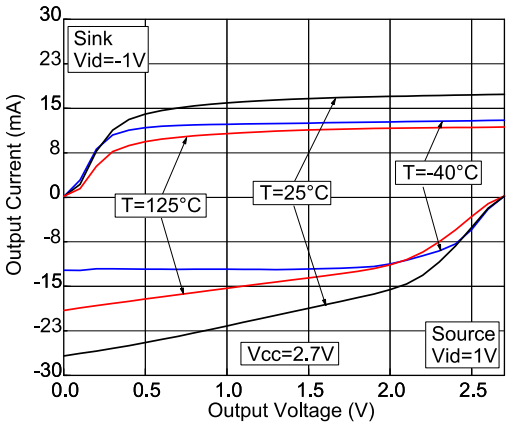


Figure 12: Output current vs. output voltage at VCC = 2.7 V



PRODUCT DATASHEET

EVEREADY

1-800-383-7323 USA/CAN
www.energizer.com

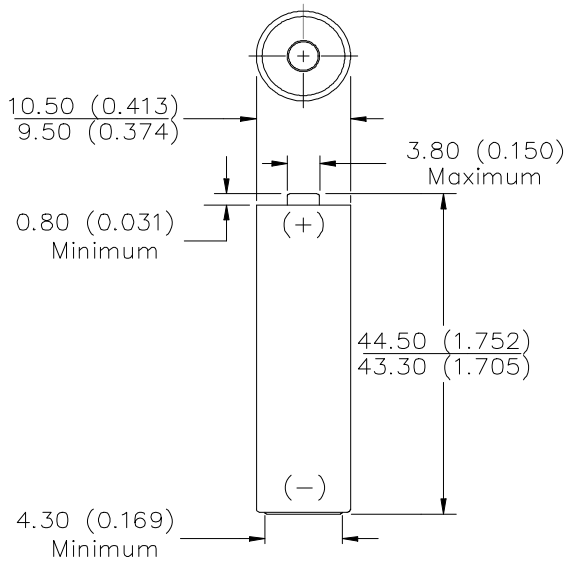
Eveready 1212

AAA
SUPER HEAVY DUTY

Chemical System:	Zinc-Manganese Dioxide (Zn/MnO_2) *(No Added Mercury or Cadmium)*
Designation:	ANSI-24D, IEC-R03
Battery Voltage:	1.5 Volts
Operating Temp:	-18ºC to 55ºC (0ºF to 130ºF)
Average Weight:	9.7 grams (0.31 oz.)
Volume:	4.0 cubic centimeters (0.2 cubic inch)
Average Capacity:	540 mAh to 0.8 volts (Rated at 25 mA continuous at 21ºC)
Cell:	One No. 12 (size "AAA")
Jacket:	Metal

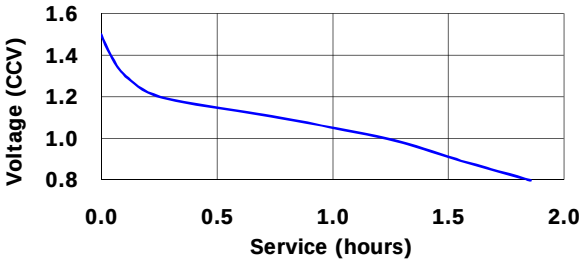
Industry Standard Dimensions

mm (inches)



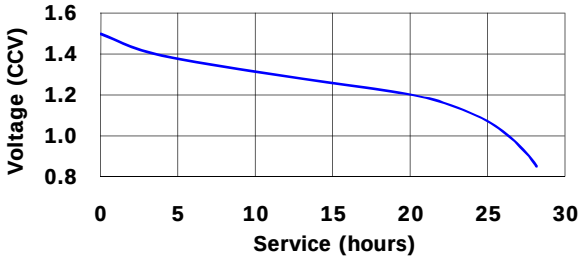
Industry Standard Test (21°C)

LIGHTING
5.1 ohm LIF

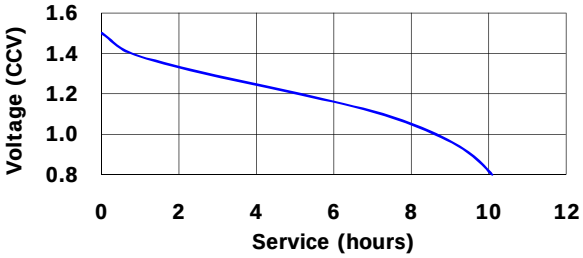


Industry Standard Tests (21°C)

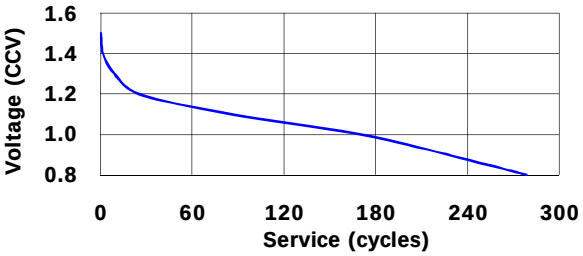
RADIO
75 ohm 4 hrs/day



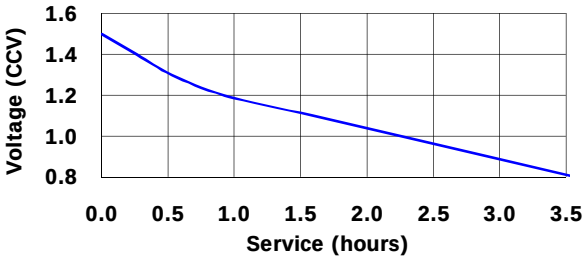
REMOTE
24 ohm 15 sec/min 8 hrs/day



PHOTOFLASH
3.6 ohm 24 hrs/day



TAPE / ELECTRONIC GAMES
10 ohm 1 hr/day



Important Notice

This data sheet contains information specific to batteries manufactured at the time of its publication.
Contents herein do not constitute a warranty.