POLITECNICO DI TORINO
ESAMI DI STATO PER L'ABILITAZIONE ALLA PROFESSIONE DI INGEGNERE
I SESSIONE 2005
Ramo Elettronica
Tema 1

L'unità elettronica di gestione di un motore termico (ciclo Otto) ha il compito di minimizzare le emissioni inquinanti e nel contempo massimizzare la potenza erogata dal motore termico ai vari regimi di rotazione. Tale obiettivo viene raggiunto mediante il controllo del titolo della miscela e dell'anticipo di accensione, sulla base delle seguenti grandezze fisiche:

- Temperatura aria al collettore di aspirazione
- Temperatura liquido refrigerante
- Angolo di apertura della farfalla
- Sensore portata aria
- Concentrazione O_2 nei gas di scarico (sonda lambda tipo HEGO)
- Numero di giri motore termico

L'unità elettronica è composta da un microprocessore, da un convertitore A/D, da opportuni circuiti di condizionamento dei segnali provenienti dai sensori oltre che da circuiti di pilotaggio degli elettro-iniettori e del circuito di accensione.

In questa sede si richiede il progetto del sistema di acquisizione dei seguenti segnali:

1. la temperatura dell'aria deve essere acquisita con una risoluzione di 0.5 °C. Le caratterisitche elettriche del sensore sono descritte in un foglio allegato.
2. la farfalla che ostruisce il collettore di aspirazione può ruotare tra 0° e 90°. La sua posizione è rilevata mediante il sensore potenziometrico di tipo differenziale (vedi figura 2). E' necessaria l'acquisizione di questo segnale con risoluzione angolare di 0.5°. Inoltre, il tempo minimo di rotazione della farfalla da 0° a 90° è di 100ms.
3. il sensore portata aria è di tipo attivo e genera un tensione proporzionale alla radice quadrata della portata. La figura 1 mostra il segnale generato da questo sensore nel caso di brusca accelerazione e decelerazione.
4. la sonda lambda è del tipo HEGO (vedi allegato) quindi la tensione di uscita è alta (0.8 V< V_{HEGO} < 1V) se la miscela è ricca (elevata concentrazione di O_2 nei gas di scarico) mentre è bassa (0.1 < V_{HEGO} < 0.2) se la miscela è magra (bassa concentrazione di O_2 nei gas di scarico).
5. il sensore di numero di giri è del tipo a riluttanza magnetica (vedi allegato)

sapendo che

a. il motore termico e' dotato di 4 cilindri e può ruotare al massimo a 6500 giri/minuto
b. ogni cilindro e' dotato di un elettro-iniettore
c. il tempo massimo di apertura di ogni elettro-iniettori e' di 500us
d. il tempo di carica della bobina di accensione e' compreso tra 1 **e** 3ms
e. il tempo massimo di elaborazione del microprocessore e' di circa 400us
f. il segnale della sonda HEGO può' essere acquisito con frequenza minima di 1 Hz
g. il funzionamento dei componenti del sistema di conversione analogico digitale e' gestito dal microprocessore.

Progettare i circuiti di condizionamento dei suddetti segnali di ingresso.

Si richiede la stesura di una relazione tecnica comprendente lo schema a blocchi, lo schema elettrico di ogni blocco e la relativa relazione di calcolo, oltre al diagramma di temporizzazione del sistema di acquisizione dei segnali.

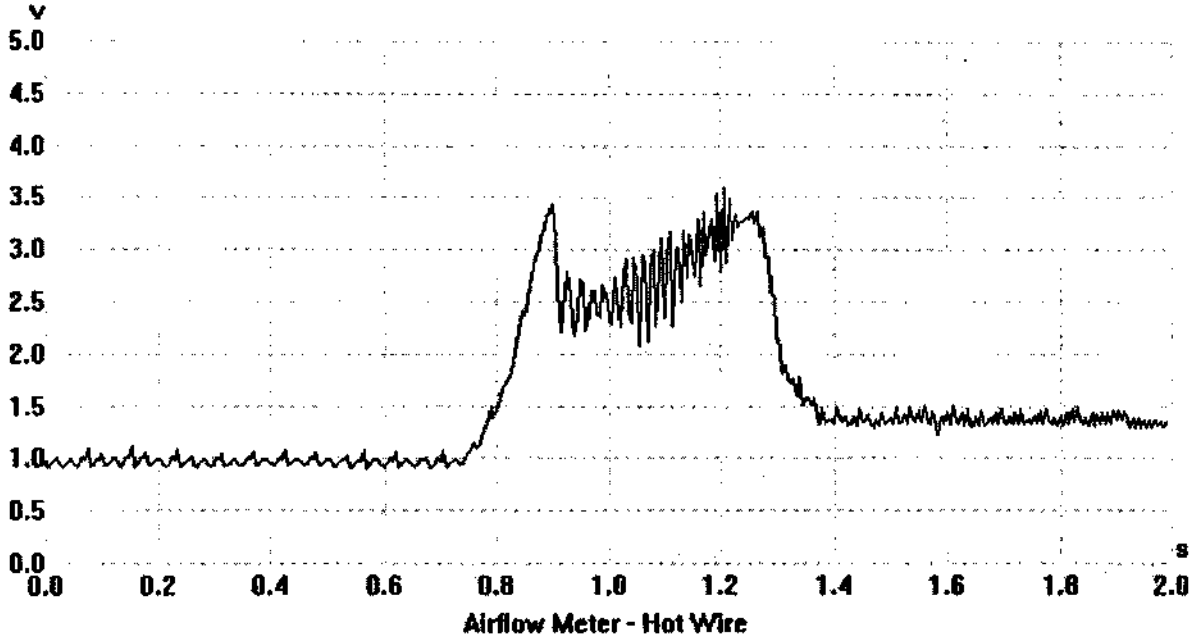


Figura 1 : tensione d'uscita del sensore di misura della portata d'aria a seguito di una accelerazione repentina e successiva deccelerazione del regime di rotazione del motore termico.

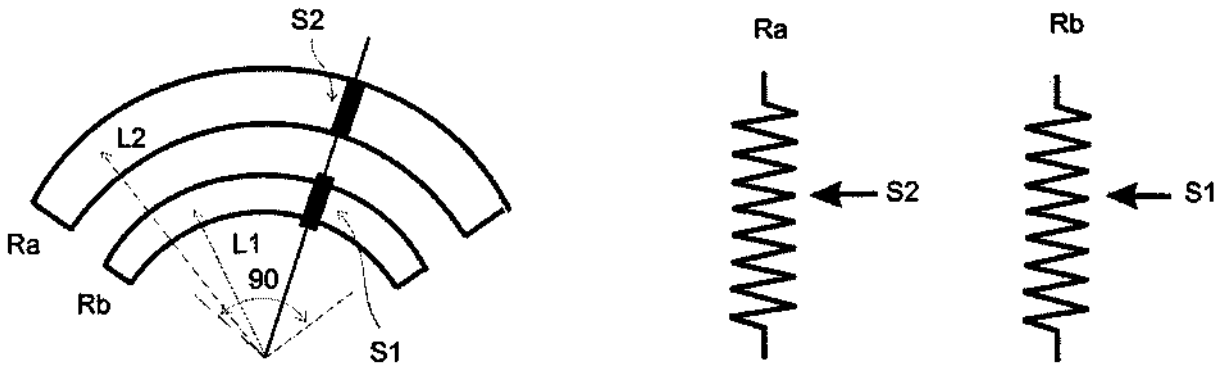


Figura 2.Resistore potenziometrico differenziale. L1= 20 mm, L2=30 mm, Sezione delle resistenze S1=S2= 1 mm^2, resistività p=50 [Ωmm].

Temperature Sensors

TD Series

GENERAL INFORMATION

TD Series temperature sensors from MICRO SWITCH respond rapidly to temperature changes, and are accurate to ±0.7°C at 20°C—completely interchangeable without recalibration. They are RTD (resistance temperature detector) sensors, and provide 8 Ω/°C sensitivity, with inherently near linear outputs.

The sensing element is a silicon chip, 0.040 × 0.050" with a thin film resistive network pattern. The chips are individually laser trimmed to provide 2000 ohms nominal resistance at room temperature (20°C), accurate to ±0.7°C. Maximum error over the entire operating range of −40 to +150°C (−40 to +302°F) is ±2.5°C. This extremely accurate trimming provides true sensor-to-sensor interchangeability without recalibration of the user circuit.

FEATURES

- Interchangeable without sensor-to-sensor recalibration
- Very small thermal mass for fast response
- Air or liquid temperature sensing
- Linear temperature sensitivity
- Proven thin film processing reliability
- Low cost
- Long term stability
- 2000 ohms nominal resistance at 20°C

TYPICAL APPLICATIONS

- HVAC – room, duct and refrigerant temperature
- Motors – overload protection
- Electronic circuits – semiconductor protection
- Process control – temperature regulation
- Automotive – air or oil temperature
- Appliances – cooking temperature

TD4A Liquid temperature sensor
TD4A liquid temperature sensor is a two-terminal threaded anodized aluminum housing. The environmentally sealed liquid temperature sensors are designed for simplicity of installation, such as in the side of a truck. TD4A sensors are not designed for total immersion. Typical response time (for one time constant) is 4 minutes in still air and 15 seconds in still water (unmounted position). The temperature rise is 0.12°C/milliwatt suspended by leads in still air, and 0.08°C/milliwatt when mounted on 1 square foot 0.25" thick aluminum foil.

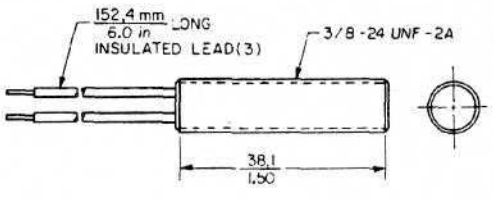
TD5A Miniature temperature sensor
The TD5A is a subminiature temperature sensor with three leads (center not connected). It has response times of 11.0 seconds and a temperature rise of .23°C per milliwatt in still air.

TD ORDER GUIDE

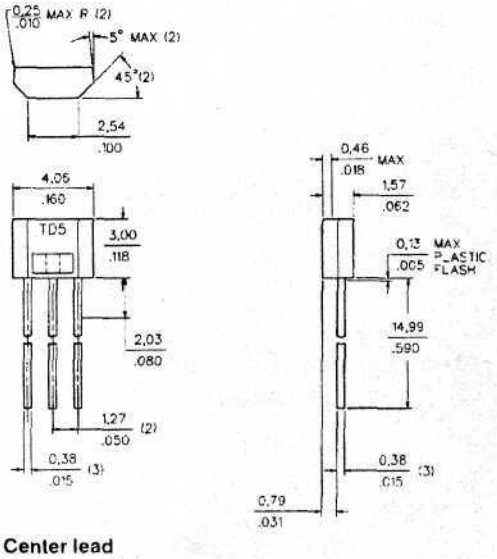
Catalog Listing	Description
TD4A	Liquid temperature sensor, 1.5° threaded (3/8-24 UNF-2A) anodized aluminum housing, two six inch black insulated leads
TD5A	Subminiature package, low cost, fast response time (TO-92)

MOUNTING DIMENSIONS (for reference only)

TD4A



TD5A



Center lead not connected

Temperature

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	−40 to +150°C (−40 to +302°F)
Storage temperature range	−55 to 165°C (−67 to +338°F)
Voltage	10 VDC Continuous (24 hours)

INTERCHANGEABILITY (with 100 mA maximum current)

Temperature	Resistance (Ohms)	Temperature	Resistance (Ohms)
−40°C (−40°F)	1584 ± 12 (1.9°C)	+60°C (140°F)	2314 ± 9 (1.1°C)
−30°C (−22°F)	1649 ± 11 (1.7°C)	+70°C (158°F)	2397 ± 10 (1.2°C)
−20°C (−4°F)	1715 ± 10 (1.5°C)	+80°C (176°F)	2482 ± 12 (1.4°C)
−10°C (14°F)	1784 ± 9 (1.3°C)	+90°C (194°F)	2569 ± 14 (1.6°C)
0°C (32°F)	1854 ± 8 (1.1°C)	+100°C (212°F)	2658 ± 16 (1.8°C)
+10°C (50°F)	1926 ± 6 (0.8°C)	+110°C (230°F)	2748 ± 18 (2.0°C)
+20°C (68°F)	2000 ± 5 (0.7°C)	+120°C (248°F)	2840 ± 19 (2.0°C)
+30°C (86°F)	2076 ± 5 (0.7°C)	+130°C (266°F)	2934 ± 21 (2.2°C)
+40°C (104°F)	2153 ± 6 (0.8°C)	+140°C (284°F)	3030 ± 23 (2.4°C)
+50°C (122°F)	2233 ± 7 (0.9°C)	+150°C (302°F)	3128 ± 25 (2.5°C)

It is recommended that resistance measurements be made at 100 μA or less to minimize internal heating of the sensor. Measurements at currents up to 1mA will not damage the sensor, but the resistance characteristics should be adjusted for internal heating.

Equation for computing resistance:

$R_T = R_O + (3.84 \times 10^{-3} \times R_O \times T) + (4.94 \times 10^{-6} \times R_O \times T^2)$

R_T = Resistance at temperature T

R_O = Resistance at 0°C

T = Temperature in °C

Figure 2
Linear Output Voltage Circuit

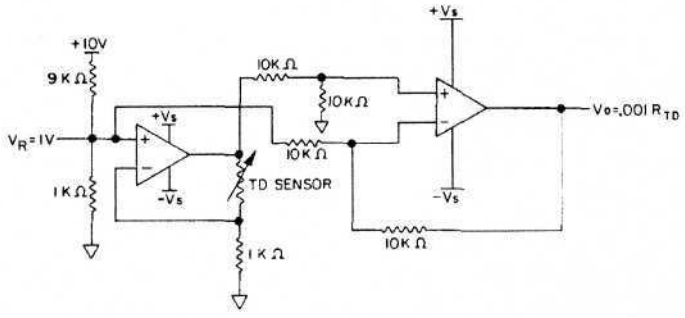
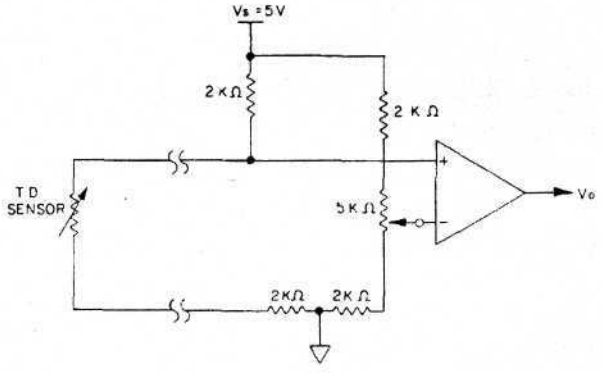


Figure 3
Adjustable Point (Comparator) Interface



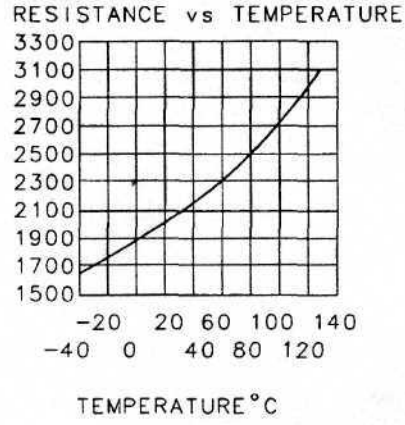
Linearity

±2% (−25 to 85°C)
±3% (−40 to 150°C)
TD sensors can be linearized to within ±0.2%.

Repeatability

±1 Ω

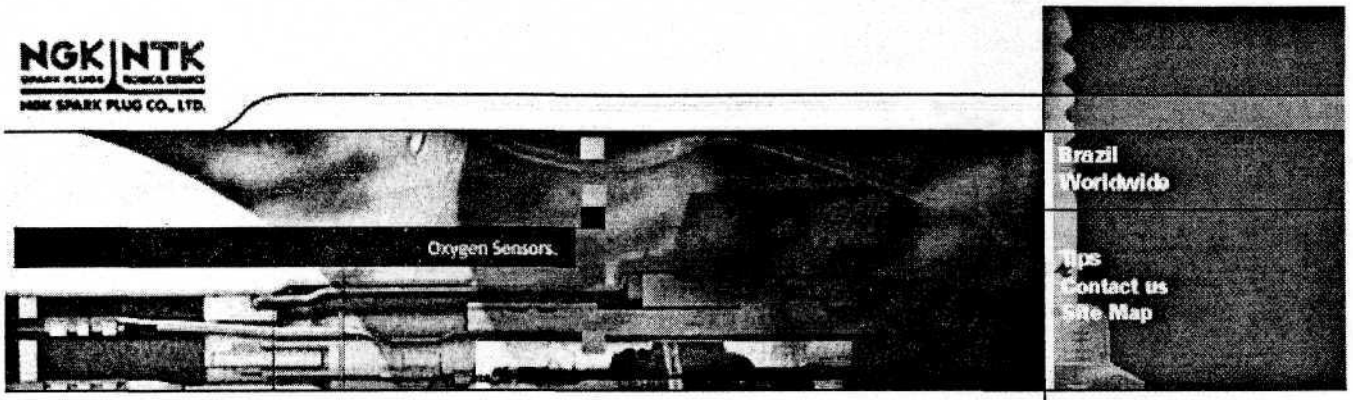
Figure 1
TD Series Resistance vs Temperature



ELECTRICAL INTERFACING

The high nominal resistance, positive temperature coefficient and linear sensitivity characteristics of the TD Series temperature sensors simplifies the task of designing the electrical interface. Figure 2 is a simple circuit that can be used to linearize the voltage output to within 0.2% or a ±0.4°C error over a range of −40° to +150°C (−40° to +302°F).

In some applications, it may be desirable to detect one particular temperature. Figure 3 illustrates one way this can be accomplished. In the comparator circuit shown, the potentiometer can be adjusted to correspond to the desired temperature.



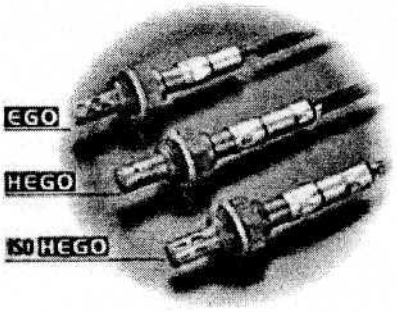
Oxygen Sensors

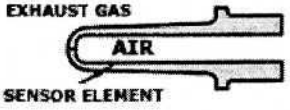
Oxygen Sensor
Zirconium Sensors
Universal Sensor
New Technology
Characteristics

Products
Spark Plugs
Ignition Cables
Oxygen Sensors
Knock Sensors
Resistor Covers
Ceramics
Tiles
Cutting Tools
Commercial Products

Zirconium Sensors

The external surface of the zirconium element is in contact with the exhaust gas; the internal surface in contact with the air. Both surfaces are covered with a fine coating of platinum.

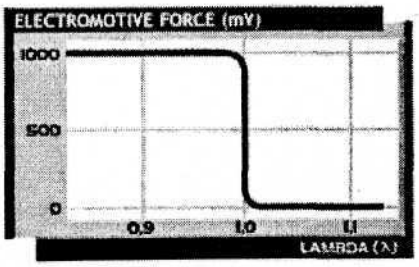




preserve the planet.
save energy.

Application Tables
Brazil

The zirconium element, at a temperature above 300°C, conducts the oxygen ions and generates electrical voltage. This electrical voltage is generated when the oxygen concentrations in the internal and external elements are different. A low voltage (near to zero) is produced when the air-fuel mixture is lean, and a voltage near 1000mV is produced when the mixture is rich.



When the air-fuel mixture nears the ideal ratio (lambda = 1), there is a sharp change in the generated voltage, from 0 to 1000mV.

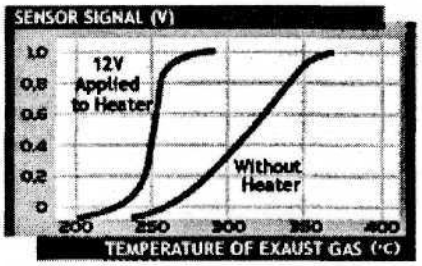
The ECU uses the voltage produced by the Lambda Sensor to instruct the mixture system to make the mixture more lean or more rich. Since the element only produces voltage when the element is above 300°C, the exhaust gas take some time to heat the element to the necessary temperature, after the engine is running. To reduce the time before the sensor begins functioning, many sensors today have an internal ceramic heater. These sensors have three or four conductive wires. NTK ceramic heaters rely on our extensive experience and ensure high performance and reliability .

Zirconium Exhaust Oxygen Sensor EGO

This sensor is highly reliable, even in conditions of extreme use, and has rapid response and is compact.

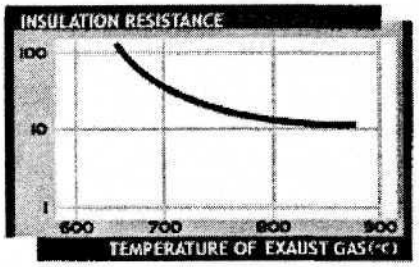
Heated Zirconium Exhaust Oxygen Sensor HEGO

A ceramic heater is inserted into the sensor, heating its interior, thus allowing it to function at a wider range of exhaust temperatures. Its characteristics vary less over time, and it begins functioning more quickly than the EGO type.



Heated Zirconium and Insulated Element Exhaust Oxygen Sensor ISO HEGO

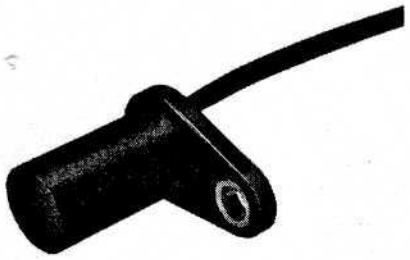
This sensor has an additional conductor to the compound signal, as well as the conventional sensor (HEGO). The stability of this signal is guaranteed by the complete insulation between the sensor element and the external metal casing, thanks to a special ceramic material.



Solid State Sensors

Hall Effect Gear Tooth Sensors

GT1 Series



TYPICAL APPLICATIONS

Automotive and Heavy Duty Vehicles:

- Camshaft and crankshaft speed/ position
- Transmission speed
- Tachometers
- Anti-skid/traction control

Industrial:

- Sprocket speed
- Chain link conveyor speed and distance
- Stop motion detector
- High speed low cost proximity
- Tachometers, Counters

FEATURES

- Senses ferrous metal targets
- Digital current sinking output (open collector)
- Better signal-to-noise ratio than variable reluctance sensors, excellent low speed performance, output amplitude not dependent on RPM
- Sensor electronically *self-adjusts* to slight variations in runout and variations in temperature, simplifying installation and maintenance
- Fast operating speed – over 100 kHz
- EMI resistant
- Reverse polarity protection and transient protection (integrated into Hall I.C.)
- Wide continuous operating temperature range (–40° to 150°C), short term to 160°C

GENERAL INFORMATION

1GT1 Series Gear Tooth Sensors use a magnetically biased Hall effect integrated circuit to accurately sense movement of ferrous metal targets. This specially designed I.C., with discrete capacitor and bias magnet, is sealed in a probe type package for physical protection and cost effective installation.

Units will function from a 4.5 to 24 VDC power supply. Output is digital, current sinking (open collector). Reverse polarity protection is standard. If power is inadvertently wired backwards, the sensor will not be damaged. Built-in protection against pulsed transients to +60V, –40V is also included.

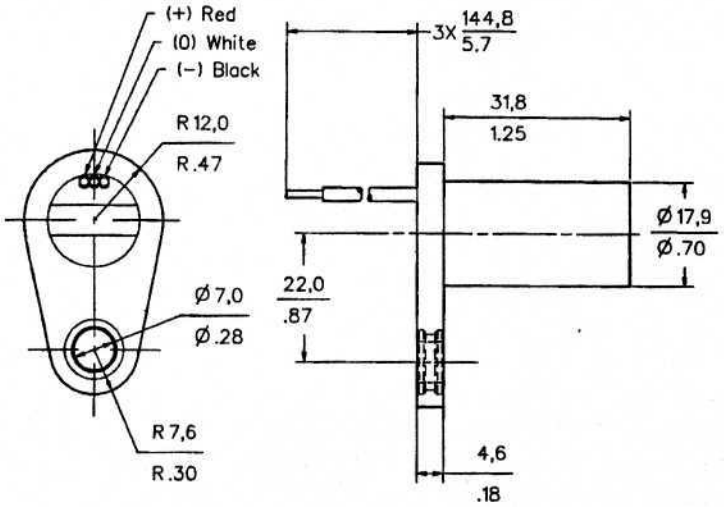
Optimum sensor performance is dependent on the following variables which must be considered in combination:

- Target material, geometry, and speed
- Sensor/target gap
- Ambient temperature
- Magnetic material in close proximity

GT1 ORDER GUIDE

Catalog Listing	Description
1GT101DC	Gear Tooth Sensor

MOUNTING DIMENSIONS (For reference only)



Solid State Sensors
Hall Effect Gear Tooth Sensors

SENSOR SPECIFICATIONS

All values were measured using 1 K pull-up resistor.

Electrical Characteristics	Supply Voltage	4.5 to 24 VDC
	Supply Current	10 mA typ., 20 mA max.
	Output Voltage (output low)	0.4 V max.
	Output Current (output high)	10 µA max. leakage into sensor
	Switching Time	
	Rise (10 to 90%)	15 µsec. max.
	Fall (90 to 10%)	1.0 µsec. max.
Absolute Maximum Ratings*	Supply Voltage (Vs)	±30 VDC continuous
	Voltage Externally Applied To Output (output high)	−0.5 to +30 V
	Output Current	40 mA sinking
	Temperature Range	
	Storage	−40 to 150° (−40 to 302°F)
	Operating	−40 to 150° C (−40 to 302°F)
Switching Characteristics**	Operate Point	3.7±1.25° (3,28±1,13 mm)
	Release Point	4.7±2.50° (4,16±2,21 mm)
	Differential Travel	8.4±3.70° (7,45±3,34 mm)

* As with all solid state components, sensor performance can be expected to deteriorate as rating limits are approached; however, sensors will not be damaged unless the limits are exceeded.
** See Reference Target table.

TARGET GUIDELINES

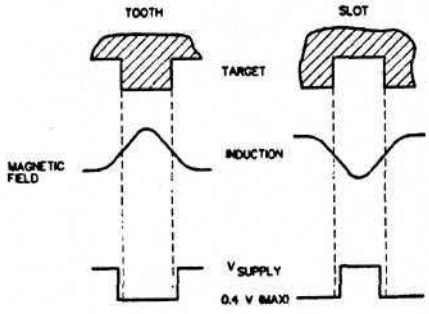
The Target Guidelines table provides basic parameters when an application is not restricted to a specific target.

Any target wheel that exceeds the following minimum specifications can be sensed over the entire temperature range of −40° to 150°C with any sensing gap up to .080 in. (2,0 mm). This data is based on a 4 in. (102 mm) diameter wheel, **rotating 10 to 3600 RPM.**

Reference Target Dimensions

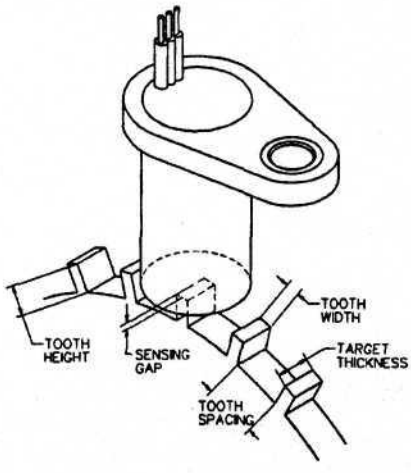
Tooth Height:	.200 in. (5,06 mm) min.
Tooth Width:	.100 in. (2,54 mm) min.
Tooth Spacing:	.400 in. (10,16 mm) min.
Target Thickness:	.250 in. (6,35 mm)

Sensor Output (with pull-up resistor added to output circuit)



REFERENCE TARGET/CONDITIONS

Characteristics will vary due to target size, geometry, location, and material. Sensor specifications were derived using a cold-rolled steel reference target. See table, right, for reference target configuration and evaluation conditions.



Target	
Diameter:	4 in. (101,6 mm)
Tooth Width:	.350 in. (8,89 mm)
Thickness:	.250 in. (6,35 mm)

Test Conditions	
Air Gap:	.040 to .080 in. (1,02 to 2,03 mm)
V Supply:	4.5 to 24 V
RPM:	10 min., 3600 max.

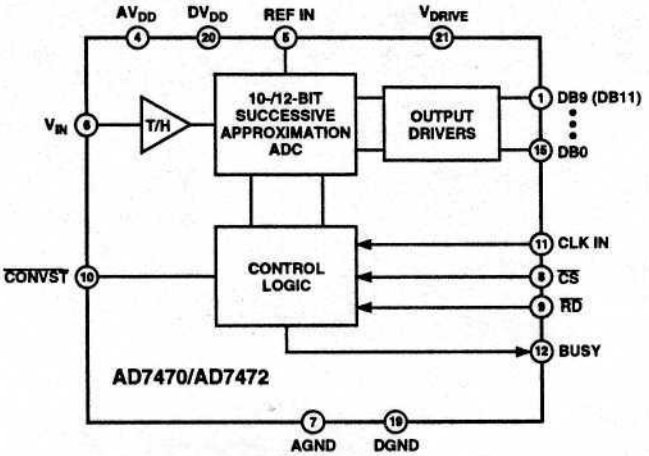
1.75 MSPS, 4 mW 10-Bit/12-Bit Parallel ADCs

AD7470/AD7472

FEATURES

Specified for V_{DD} of 2.7 V to 5.25 V
1.75 MSPS for AD7470 (10-Bit)
1.5 MSPS for AD7472 (12-Bit)
Low Power
AD7470: 3.34 mW Typ at 1.5 MSPS with 3 V Supplies
7.97 mW Typ at 1.75 MSPS with 5 V Supplies
AD7472: 3.54 mW Typ at 1.2 MSPS with 3 V Supplies
8.7 mW Typ at 1.5 MSPS with 5 V Supplies
Wide Input Bandwidth
70 dB Typ SNR at 500 kHz Input Frequency
Flexible Power/Throughput Rate Management
No Pipeline Delays
High Speed Parallel Interface
Sleep Mode: 50 nA Typ
24-Lead SOIC and TSSOP Packages

FUNCTIONAL BLOCK DIAGRAM



AD7470 IS A 10-BIT PART WITH DB0 TO DB9 AS OUTPUTS.
AD7472 IS A 12-BIT PART WITH DB0 TO DB11 AS OUTPUTS.

GENERAL DESCRIPTION

The AD7470/AD7472 are 10-bit/12-bit high speed, low power, successive approximation ADCs. The parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates up to 1.5 MSPS for the 12-bit AD7472 and up to 1.75 MSPS for the 10-bit AD7470. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

The conversion process and data acquisition are controlled using standard control inputs, allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{\text{CONVST}}$, and conversion is also initiated at this point. BUSY goes high at the start of conversion and goes low 531.66 ns after falling edge of $\overline{\text{CONVST}}$ (AD7472 with a clock frequency of 26 MHz) to indicate that the conversion is complete. There are no pipeline delays associated with the parts. The conversion result is accessed via standard $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals over a high speed parallel interface.

The AD7470/AD7472 use advanced design techniques to achieve very low power dissipation at high throughput rates. With 3 V supplies and 1.5 MSPS throughput rates, the AD7470 typically consumes, on average, just 1.1 mA. With 5 V supplies and 1.75 MSPS, the average current consumption is typically 1.6 mA. The part also offers flexible power/throughput rate management. Operating the AD7470 with 3 V supplies and 500 kSPS throughput reduces the current consumption to 713 μA. At 5 V supplies and 500 kSPS, the part consumes 944 μA.

It is also possible to operate the parts in an auto sleep mode, where the part wakes up to do a conversion and automatically enters sleep mode at the end of conversion. This method allows very low power dissipation numbers at lower throughput rates. In this mode, the AD7472 can be operated with 3 V supplies at 100 kSPS, and consume an average current of just 124 μA. At 5 V supplies and 100 kSPS, the average current consumption is 171 μA.

The analog input range for the part is 0 V to REF IN. The 2.5 V reference is applied externally to the REF IN pin. The conversion rate is determined by the externally-applied clock.

PRODUCT HIGHLIGHTS

1. High Throughput with Low Power Consumption. The AD7470 offers 1.75 MSPS throughput and the AD7472 offers 1.5 MSPS throughput rates with 4 mW power consumption.
2. Flexible Power/Throughput Rate Management. The conversion rate is determined by an externally-applied clock allowing the power to be reduced as the conversion rate is reduced. The part also features an auto sleep mode to maximize power efficiency at lower throughput rates.
3. No Pipeline Delay. The part features a standard successive approximation ADC with accurate control of the sampling instant via a $\overline{\text{CONVST}}$ input and once off conversion control.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD7470–SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V[2], REF IN = 2.5 V, f_{CLKIN} = 30 MHz @ 5 V and 24 MHz @ 3 V; $T_A = T_{MIN}$ to T_{MAX}[3], unless otherwise noted.)

Parameter	A Version[1]		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE	5 V	3 V		f_S = 1.75 MSPS @ 5 V, f_S = 1.5 MSPS @ 3 V
Signal to Noise + Distortion (SINAD)	60	60	dB min	f_{IN} = 500 kHz Sine Wave
	60	60	dB min	f_{IN} = 100 kHz Sine Wave
Signal-to-Noise Ratio (SNR)	60	60	dB min	f_{IN} = 500 kHz Sine Wave
	60	60	dB min	f_{IN} = 100 kHz Sine Wave
Total Harmonic Distortion (THD)	–83	–83	dB typ	f_{IN} = 500 kHz Sine Wave
	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR)	–85	–85	dB typ	f_{IN} = 500 kHz Sine Wave
	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Intermodulation Distortion (IMD)				
Second-Order Terms	–79	–75	dB typ	f_{IN} = 500 kHz Sine Wave
	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Third-Order Terms	–77	–75	dB typ	f_{IN} = 500 kHz Sine Wave
	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Aperture Delay	5	5	ns typ	
Aperture Jitter	15	15	ps typ	
Full Power Bandwidth	20	20	MHz typ	@ 3 dB
DC ACCURACY				f_S = 1.75 MSPS @ 5 V; f_S = 1.5 MSPS @ 3 V
Resolution	10	10	Bits	
Integral Nonlinearity	±1	±1	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error	±2.5	±2.5	LSB max	
Gain Error	±1	±1	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN	0 to REF IN	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	33	33	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	2.5	V	±1% for Specified Performance
DC Leakage Current	±1	±1	µA max	
Input Capacitance	10/20	10/20	pF typ	Track-and-Hold Mode
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[4]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	12	12	CLK IN Cycles (max)	
Track-and-Hold Acquisition Time	135	135	ns min	
Throughput Rate	1.75	1.5	MSPS max	Conversion Time + Acquisition Time CLK IN of 30 MHz @ 5 V and 24 MHz @ 3 V
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25		V min/max	
I_{DD}[5]				Digital Inputs = 0 V or DV_{DD}
Normal Mode	2.4		mA max	V_{DD} = 4.75 V to 5.25 V; f_S = 1.75 MSPS; Typ 2 mA
Quiescent Current	900		µA max	V_{DD} = 4.75 V to 5.25 V; f_S = 1.75 MSPS
Normal Mode	1.5		mA max	V_{DD} = 2.7 V to 3.3 V; f_S = 1.5 MSPS; Typ 1.3 mA
Quiescent Current	800		µA max	V_{DD} = 2.7 V to 3.3 V; f_S = 1.5 MSPS
Sleep Mode	1		µA max	CLK IN = 0 V or DV_{DD}
Power Dissipation[5]				Digital Inputs = 0 V or DV_{DD}
Normal Mode	12		mW max	V_{DD} = 5 V
	4.5		mW max	V_{DD} = 3 V
Sleep Mode	5		µW max	V_{DD} = 5 V; CLK IN = 0 V or DV_{DD}
	3		µW max	V_{DD} = 3 V; CLK IN = 0 V or DV_{DD}

NOTES

[1]Temperature ranges as follows: A Version: –40°C to +85°C.

[2]The AD7470 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 59 dB; THD (100 kHz) = –84 dB; INL ±0.8 LSB.

[3]The AD7470 will typically maintain A-grade performance up to 125°C, with a reduced CLK of 20 MHz @ 5 V and 16 MHz @ 3 V. Typical sleep mode current @ 125°C is 700 nA.

[4]Sample tested @ 25°C to ensure compliance.

[5]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7472–SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V[2], REF IN = 2.5 V, A and B Versions: f_{CLKIN} = 26 MHz @ 5 V and 20 MHz @ 3 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]		B Version[1]		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE	5 V	3 V	5 V	3 V		f_S = 1.5 MSPS @ 5 V, f_S = 1.2 MSPS @ 3 V
Signal to Noise + Distortion (SINAD)	69	69	69	69	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Signal-to-Noise Ratio (SNR)	70	70	70	70	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Total Harmonic Distortion (THD)	–83	–78	–83	–78	dB typ	f_{IN} = 500 kHz Sine Wave
	–83	–84	–83	–84	dB typ	f_{IN} = 100 kHz Sine Wave
	–75	–75	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR)	–86	–81	–86	–81	dB typ	f_{IN} = 500 kHz Sine Wave
	–86	–86	–86	–86	dB typ	f_{IN} = 100 kHz Sine Wave
	–76	–76	–76	–76	dB max	f_{IN} = 100 kHz Sine Wave
Intermodulation Distortion (IMD)						
Second-Order Terms	–77	–77	–77	–77	dB typ	f_{IN} = 500 kHz Sine Wave
	–86	–86	–86	–86	dB typ	f_{IN} = 100 kHz Sine Wave
Third-Order Terms	–77	–77	–77	–77	dB typ	f_{IN} = 500 kHz Sine Wave
	–86	–86	–86	–86	dB typ	f_{IN} = 100 kHz Sine Wave
Aperture Delay	5	5	5	5	ns typ	
Aperture Jitter	15	15	15	15	ps typ	
Full Power Bandwidth	20	20	20	20	MHz typ	@ 3 dB
DC ACCURACY						f_S = 1.5 MSPS @ 5 V, f_S = 1.2 MSPS @ 3 V
Resolution	12	12	12	12	Bits	
Integral Nonlinearity	±2	±2	±1	±1	LSB max	Guaranteed No Missed Codes to 11 Bits (A Version)
Differential Nonlinearity	±1.8	±1.8	±0.9	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits (B Version)
Offset Error	±10	±10	±10	±10	LSB max	
Gain Error	±2	±2	±2	±2	LSB max	
ANALOG INPUT						
Input Voltage Ranges	0 to REF IN	0 to REF IN	0 to REF IN	0 to REF IN	V	
DC Leakage Current	±1	±1	±1	±1	μA max	
Input Capacitance	33	33	33	33	pF typ	
REFERENCE INPUT						
REF IN Input Voltage Range	2.5	2.5	2.5	2.5	V	±1% for Specified Performance
DC Leakage Current	±1	±1	±1	±1	μA max	
Input Capacitance	10/20	10/20	10/20	10/20	pF typ	Track-and-Hold Mode
LOGIC INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	±1	±1	μA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	10	10	10	pF max	
LOGIC OUTPUTS						
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	0.4	V max	I_{SINK} = 200 μA
Floating-State Leakage Current	±10	±10	±10	±10	μA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	10	10	10	pF max	
Output Coding	Straight (Natural) Binary		Straight (Natural) Binary			
CONVERSION RATE						
Conversion Time	14	14	14	14	CLK IN Cycles (max)	
Track-and-Hold Acquisition Time	135	135	135	135	ns min	
Throughput Rate	1.5	1.2	1.5	1.2	MSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS						
V_{DD}	+2.7/+5.25		+2.7/+5.25		V min/max	
I_{DD}[4]						Digital Inputs = 0 V or DV_{DD}
Normal Mode	2.4		2.4		mA max	V_{DD} = 4.75 V to 5.25 V; Typ 2 mA; f_S = 1.5 MSPS
Quiescent Current	900		900		μA max	V_{DD} = 4.75 V to 5.25 V; f_S = 1.5 MSPS
Normal Mode	1.5		1.5		mA max	V_{DD} = 2.7 V to 3.3 V; Typ 1.3 mA; f_S = 1.2 MSPS
Quiescent Current	800		800		μA max	V_{DD} = 2.7 V to 3.3 V; f_S = 1.2 MSPS
Sleep Mode	1		1		μA max	CLK IN = 0 V or DV_{DD}
Power Dissipation[4]						Digital Inputs = 0 V or DV_{DD}
Normal Mode	12		12		mW max	V_{DD} = 5 V
	4.5		4.5		mW max	V_{DD} = 3 V
Sleep Mode	5		5		μW max	V_{DD} = 5 V; CLK IN = 0 V or DV_{DD}
	3		3		μW max	V_{DD} = 3 V; CLK IN = 0 V or DV_{DD}

NOTES

[1]Temperature ranges as follows: A and B Versions: –40°C to +85°C.

[2]The AD7472 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 68 dB; THD (100 kHz) = –84 dB; INL ±0.8 LSB.

[3]Sample tested @ 25°C to ensure compliance.

[4]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7472–SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V[2], REF IN = 2.5 V, Y Version: f_{CLKIN} = 20 MHz @ 5 V and 14 MHz @ 3 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Y Version[1]		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE	5 V	3 V		f_S = 1.2 MSPS @ 5 V, f_S = 875 kSPS @ 3 V
Signal to Noise + Distortion (SINAD)	69	69	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Signal-to-Noise Ratio (SNR)	70	70	dB typ	f_{IN} = 500 kHz Sine Wave
	68	68	dB min	f_{IN} = 100 kHz Sine Wave
Total Harmonic Distortion (THD)	–83	–78	dB typ	f_{IN} = 500 kHz Sine Wave
	–83	–84	dB typ	f_{IN} = 100 kHz Sine Wave
	–75	–75	dB max	f_{IN} = 100 kHz Sine Wave
Peak Harmonic or Spurious Noise (SFDR)	–86	–81	dB typ	f_{IN} = 500 kHz Sine Wave
	–86	–86	dB typ	f_{IN} = 100 kHz Sine Wave
	–76	–76	dB max	f_{IN} = 100 kHz Sine Wave
Intermodulation Distortion (IMD)				
Second-Order Terms	–77	–77	dB typ	f_{IN} = 500 kHz Sine Wave
	–86	–86	dB typ	f_{IN} = 100 kHz Sine Wave
Third-Order Terms	–77	–77	dB typ	f_{IN} = 500 kHz Sine Wave
	–86	–86	dB typ	f_{IN} = 100 kHz Sine Wave
Aperture Delay	5	5	ns typ	
Aperture Jitter	15	15	ps typ	
Full Power Bandwidth	20	20	MHz typ	@ 3 dB
DC ACCURACY				f_S = 1.2 MSPS @ 5 V; f_S = 875 kSPS @ 3 V
Resolution	12	12	Bits	
Integral Nonlinearity	±2	±2	LSB max	
Differential Nonlinearity	±1.8	±1.8	LSB max	Guaranteed No Missed Codes to 11 Bits
Offset Error	±10	±10	LSB max	
Gain Error	±2	±2	LSB max	
ANALOG INPUT				
Input Voltage Ranges	0 to REF IN	0 to REF IN	V	
DC Leakage Current	±1	±1	µA max	
Input Capacitance	33	33	pF typ	
REFERENCE INPUT				
REF IN Input Voltage Range	2.5	2.5	V	±1% for Specified Performance
DC Leakage Current	±1	±1	µA max	
Input Capacitance	10/20	10/20	pF typ	Track-and-Hold Mode
LOGIC INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.4	0.4	V max	
Input Current, I_{IN}	±1	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Capacitance, C_{IN}[3]	10	10	pF max	
LOGIC OUTPUTS				
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2	V_{DRIVE} – 0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±10	±10	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	10	pF max	
Output Coding	Straight (Natural) Binary			
CONVERSION RATE				
Conversion Time	14	14	CLK IN Cycles (max)	
Track-and-Hold Acquisition Time	140	140	ns min	
Throughput Rate	1200	875	kSPS max	Conversion Time + Acquisition Time
POWER REQUIREMENTS				
V_{DD}	+2.7/+5.25		V min/max	
I_{DD}[4]				Digital Inputs = 0 V or DV_{DD}
Normal Mode	2.4		mA max	V_{DD} = 4.75 V to 5.25 V; f_S = 1.2 MSPS; Typ 2 mA
Quiescent Current	900		µA max	V_{DD} = 4.75 V to 5.25 V; f_S = 1.2 MSPS
Normal Mode	1.5		mA max	V_{DD} = 2.7 V to 3.3 V; f_S = 875 kSPS; Typ 1.3 mA
Quiescent Current	800		µA max	V_{DD} = 2.7 V to 3.3 V; f_S = 875 kSPS
Sleep Mode	2		µA max	CLK IN = 0 V or DV_{DD}
Power Dissipation[4]				Digital Inputs = 0 V or DV_{DD}
Normal Mode	12		mW max	V_{DD} = 5 V
	4.5		mW max	V_{DD} = 3 V
Sleep Mode	10		µW max	V_{DD} = 5 V; CLK IN = 0 V or DV_{DD}
	6		µW max	V_{DD} = 3 V; CLK IN = 0 V or DV_{DD}

NOTES

[1]Temperature ranges as follows: Y Version: –40°C to +125°C.

[2]The AD7472 functionally works at 2.35 V. Typical specifications @ 25°C for SNR (100 kHz) = 68 dB; THD (100 kHz) = –84 dB; INL ±0.8 LSB.

[3]Sample tested @ 25°C to ensure compliance.

[4]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

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TIMING SPECIFICATIONS[1] (V_{DD} = 2.7 V to 5.25 V, REF IN = 2.5 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7470	AD7472	Unit	Description
f_{CLK}[2]	10	10	kHz min	
	30	26	MHz max	
$t_{CONVERT}$	436.42	531.66	ns min	$t_{CLK} = 1/f_{CLK\ IN}$
t_{WAKEUP}	1	1	μs max	Wake-Up Time
t_1	10	10	ns min	$\overline{CONVST}$ Pulse Width
t_2				$\overline{CONVST}$ to BUSY Delay,
	10	10	ns max	V_{DD} = 5 V, A and B Versions
		15	ns max	V_{DD} = 5 V, Y Version
	30	30	ns max	V_{DD} = 3 V, A and B Versions
		35	ns max	V_{DD} = 3 V, Y Version
t_3	0	0	ns max	BUSY to $\overline{CS}$ Setup Time
t_4[3]	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_5	20	20	ns min	$\overline{RD}$ Pulse Width
t_6[3]	15	15	ns min	Data Access Time After Falling Edge of $\overline{RD}$
t_7[4]	8	8	ns max	Bus Relinquish Time After Rising Edge of $\overline{RD}$
t_8	0	0	ns max	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_9				Acquisition Time
	135	135	ns max	A and B Versions
		140	ns max	Y Version
t_{10}	100	100	ns min	Quiet Time

NOTES

[1]Sample tested at 25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V. See Figure 1.

[2]Mark/Space ratio for the CLK inputs is 40/60 to 60/40. First CLK pulse should be 10 ns min from falling edge of $\overline{CONVST}$.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_7 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_7, quoted in the timing characteristics, is the true bus relinquish time of the part and is independent of the bus loading.

Specifications subject to change without notice.

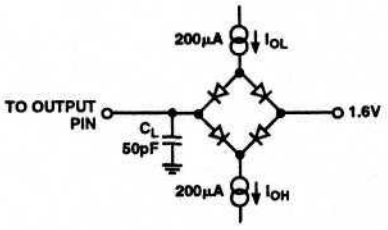

Figure 1. Load Circuit for Digital Output Timing Specifications

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ABSOLUTE MAXIMUM RATINGS[1]
(T_A = 25°C unless otherwise noted.)

AV_{DD} to AGND/DGND ..... –0.3 V to +7 V
DV_{DD} to AGND/DGND ..... –0.3 V to +7 V
V_{DRIVE} to AGND/DGND ..... –0.3 V to +7 V
AV_{DD} to DV_{DD} ..... –0.3 V to +0.3 V
V_{DRIVE} to DV_{DD} ..... –0.3 V to DV_{DD} + 0.3 V
AGND to DGND ..... –0.3 V to +0.3 V
Analog Input Voltage to AGND .... –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND .... –0.3 V to DV_{DD} + 0.3 V
REF IN to AGND ..... –0.3 V to AV_{DD} + 0.3 V
Input Current to Any Pin Except Supplies[2] ..... ±10 mA
Operating Temperature Range
  Commercial (A and B Versions) ..... –40°C to +85°C
  Industrial (Y Version) ..... –40°C to +125°C
  Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
  θ_{JA} Thermal Impedance ..... 75°C/W (SOIC)
  .....115°C/W (TSSOP)
  θ_{JC} Thermal Impedance ..... 25°C/W (SOIC)
  ..... 35°C/W (TSSOP)
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C
ESD .....1.5 kV

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch-up.

ORDERING GUIDE

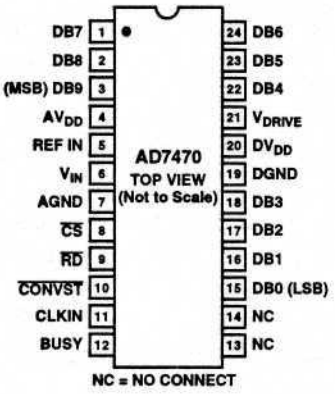
Model	Temperature Range	Resolution (Bits)	Package Options[1]	Package Description
AD7470ARU	–40°C to +85°C	10	RU-24	TSSOP
AD7470ARU-REEL	–40°C to +85°C	10	RU-24	TSSOP
AD7470ARU-REEL7	–40°C to +85°C	10	RU-24	TSSOP
AD7472AR	–40°C to +85°C	12	R-24	SOIC
AD7472AR-REEL	–40°C to +85°C	12	R-24	SOIC
AD7472AR-REEL7	–40°C to +85°C	12	R-24	SOIC
AD7472ARU	–40°C to +85°C	12	RU-24	TSSOP
AD7472ARU-REEL	–40°C to +85°C	12	RU-24	TSSOP
AD7472ARU-REEL7	–40°C to +85°C	12	RU-24	TSSOP
AD7472BR	–40°C to +85°C	12	R-24	SOIC
AD7472BR-REEL	–40°C to +85°C	12	R-24	SOIC
AD7472BRU	–40°C to +85°C	12	RU-24	TSSOP
AD7472BRU-REEL	–40°C to +85°C	12	RU-24	TSSOP
AD7472BRU-REEL7	–40°C to +85°C	12	RU-24	TSSOP
AD7472YR	–40°C to +125°C	12	R-24	SOIC
AD7472YR-REEL	–40°C to +125°C	12	R-24	SOIC
AD7472YRU	–40°C to +125°C	12	RU-24	TSSOP
AD7472YRU-REEL	–40°C to +125°C	12	RU-24	TSSOP
AD7472YRU-REEL7	–40°C to +125°C	12	RU-24	TSSOP
EVAL-AD7470CB[2]				Evaluation Board
EVAL-AD7472CB[2]				Evaluation Board
EVAL CONTROL BRD2[3]				Controller Board

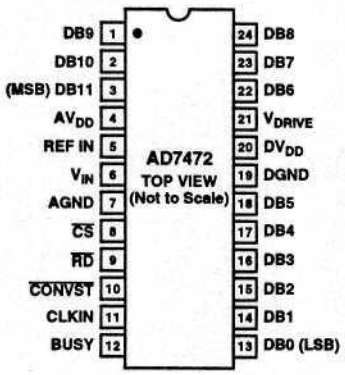
NOTES
[1]R = SOIC; RU = TSSOP.
[2]This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, you need to order the specific ADC evaluation board, for example, EVAL-AD7472CB, the EVAL CONTROL BRD2, and a 12 V ac transformer. See the relevant evaluation board application note for more information.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7470/AD7472 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS





PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input used in conjunction with $\overline{RD}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to the same AND gate on the input so the signals are interchangeable. $\overline{CS}$ can be hardwired permanently low.
$\overline{RD}$	Read Input. Logic input used in conjunction with $\overline{CS}$ to access the conversion result. The conversion result is placed on the data bus following the falling edge of both $\overline{CS}$ and $\overline{RD}$. $\overline{CS}$ and $\overline{RD}$ are both connected to same AND gate on the input so the signals are interchangeable. $\overline{CS}$ and $\overline{RD}$ can be hardwired permanently low, in which case the data bus is always active and the result of the new conversion is clocked out slightly before to the BUSY line going low.
$\overline{CONVST}$	Conversion Start Input. Logic input used to initiate conversion. The input track-and-hold amplifier goes from track mode to hold mode on the falling edge of $\overline{CONVST}$, and the conversion process is initiated at this point. The conversion input can be as narrow as 10 ns. If the $\overline{CONVST}$ input is kept low for the duration of conversion and is still low at the end of conversion, the part will automatically enter sleep mode. If the part enters this sleep mode, the next rising edge of $\overline{CONVST}$ wakes up the part. Wake-up time for the part is typically 1 µs.
CLK IN	Master Clock Input. The clock source for the conversion process is applied to this pin. Conversion time for the AD7472 takes 14 clock cycles, and conversion time for the AD7470 takes 12 clock cycles. The frequency of this master clock input, therefore, determines the conversion time and achievable throughput rate. While the ADC is not converting, the clock-in pad is in three-state and thus no clock is going through the part.
BUSY	BUSY Output. Logic output indicating the status of the conversion process. The BUSY signal goes high after the falling edge of $\overline{CONVST}$ and stays high for the duration of conversion. Once conversion is complete and the conversion result is in the output register, the BUSY line returns low. The track-and-hold returns to track mode just prior to the falling edge of BUSY, and the acquisition time for the part begins when BUSY goes low. If the $\overline{CONVST}$ input is still low when BUSY goes low, the part automatically enters its sleep mode on the falling edge of BUSY.
REF IN	Reference Input. An external reference must be applied to this input. The voltage range for the external reference is 2.5 V ±1% for specified performance.
AV_{DD}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the only supply voltage for all analog circuitry on the AD7470/AD7472. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to AGND.
DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD7470/AD7472 aside from the output drivers. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.
AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7470/AD7472. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis.

PIN FUNCTION DESCRIPTIONS (continued)

Mnemonic	Function
DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7470 and AD7472. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to REF IN. The analog input presents a high dc input impedance.
V_{DRIVE}	Supply Voltage for the Output Drivers, 2.7 V to 5.25 V. This voltage determines the output high voltage for the data output pins. It allows AV_{DD} and DV_{DD} to operate at 5 V (and maximize the dynamic performance of the (ADC), while the digital outputs can interface to 3 V logic.
DB0–DB9/11	Data Bit 0 to Data Bit 9 (AD7470) and DB11 (AD7472). Parallel digital outputs that provide the conversion result for the part. These are three-state outputs that are controlled by $\overline{CS}$ and $\overline{RD}$. The output high voltage level for these outputs is determined by the V_{DRIVE} input.

PARALLEL INTERFACE

The parallel interfaces of the AD7470 and AD7472 are 10 bits and 12 bits wide, respectively. The output data buffers are activated when both $\overline{CS}$ and $\overline{RD}$ are logic low. At this point, the contents of the data register are placed onto the data bus. Figure 10 shows the timing diagram for the parallel port.

Figure 11 shows the timing diagram for the parallel port when $\overline{CS}$ and $\overline{RD}$ are tied permanently low. In this setup, once BUSY line goes from high to low, the conversion process is completed. The data is available on the output bus slightly before the falling edge of BUSY.

It is important to point out that data bus cannot change state while the ADC is doing a conversion as this would have a detrimental effect on the conversion in progress. The data out lines will go three-state again when either the $\overline{RD}$ or the $\overline{CS}$ line goes high. Thus the $\overline{CS}$ can be tied low permanently, leaving the $\overline{RD}$ line to control conversion result access. Refer to V_{DRIVE} section for output voltage levels.

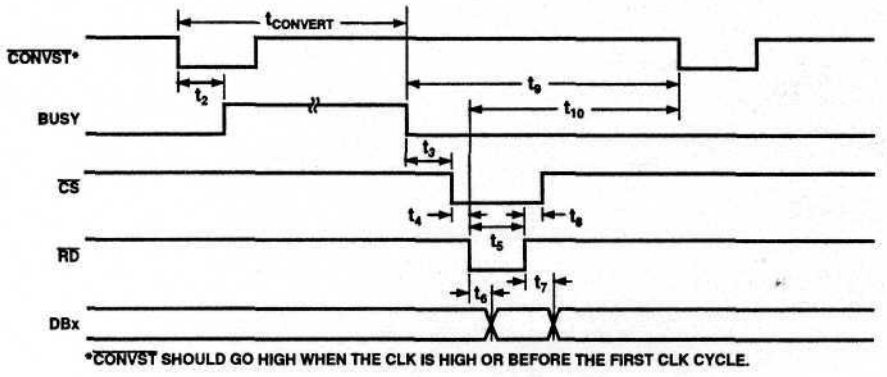


Figure 10. Parallel Port Timing

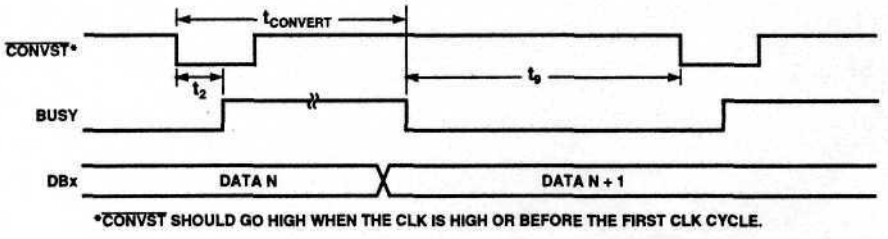


Figure 11. Parallel Port Timing with $\overline{CS}$ and $\overline{RD}$ Tied Low

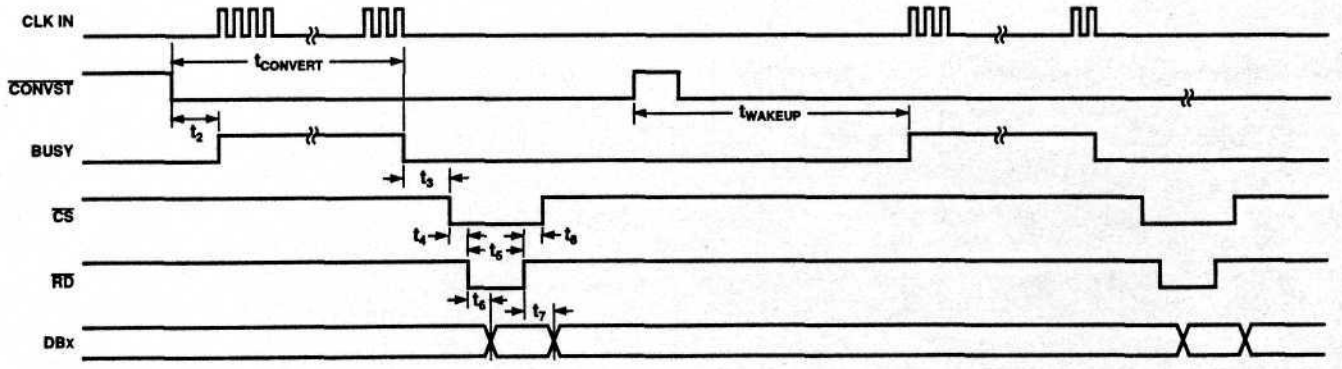


Figure 12. Wake-Up Timing Diagram (Burst Clock)

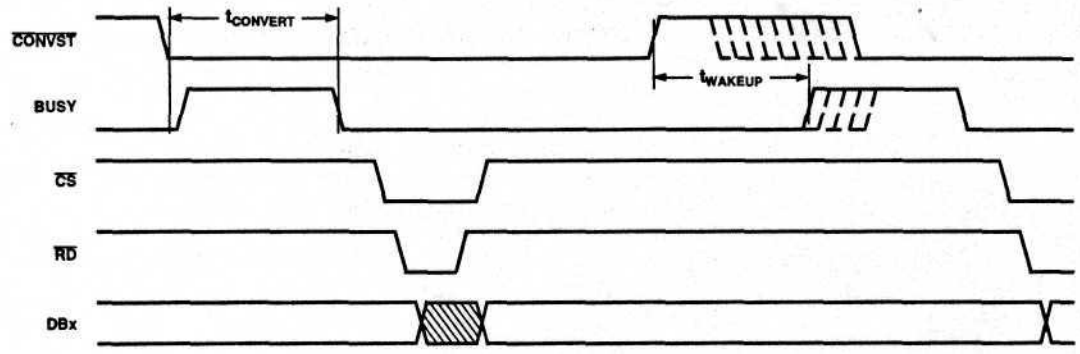


Figure 13. Mode 2 Operation

OPERATING MODES

The AD7470 and AD7472 have two possible modes of operation, depending on the state of the $\overline{\text{CONVST}}$ pulse at the end of a conversion, Mode 1 and Mode 2. There is a continuous clock on the CLKIN pin.

Mode 1 (High Speed Sampling)

In this mode of operation, the $\overline{\text{CONVST}}$ pulse is brought high before the end of conversion i.e., before BUSY goes low (see Figure 10). If the $\overline{\text{CONVST}}$ pin is brought from high to low while BUSY is high, the conversion is restarted. When operating in this mode, a new conversion should not be initiated until the acquisition time has elapsed after BUSY goes low. This acquisition time allows the track-and-hold circuit to accurately acquire the input signal. As mentioned earlier, a read should not be done during a conversion. This mode facilitates the fastest throughput times for the AD7470/AD7472.

Mode 2 (Sleep Mode)

Figure 13 shows AD7470/AD7472 in Mode 2 operation where the ADC goes into sleep mode after conversion. The $\overline{\text{CONVST}}$ line is brought low to initiate a conversion and remains low until after the end of conversion. If $\overline{\text{CONVST}}$ goes high and low again while BUSY is high, the conversion is restarted. Once the BUSY line goes from a high to a low, the $\overline{\text{CONVST}}$ line has its status checked and, if low, the part enters sleep mode.

The device wakes up again on the rising edge of the $\overline{\text{CONVST}}$ signal. There is a wake-up time of typically 1 μs after the rising edge of $\overline{\text{CONVST}}$ before the BUSY line can go high to indicate start of conversion. BUSY will only go high once $\overline{\text{CONVST}}$ goes low. The $\overline{\text{CONVST}}$ line can go from a high to a low during this wake-up time, but the conversion will still not be initiated until after the 1 μs wake-up time. Superior power performance can be achieved in this mode of operation by waking up the AD7470 and AD7472 only to carry out a conversion.

Burst Mode

Burst mode on the AD7470/AD7472 is a subsection of Mode 1 and Mode 2; the clock is noncontinuous. Figure 12 shows how the ADC works in burst mode for Mode 2. The clock needs to be switched on only during conversion, a minimum of 12 clock cycles for the AD7470 and 14 clock cycles for the AD7472. Because the clock is off during nonconverting intervals, system power is saved. The BUSY signal can be used to gate the CLKIN pulses. The ADC does not begin the conversion process until the first CLKIN rising edge after BUSY goes high. The clock needs to start less than two clock cycles away from the $\overline{\text{CONVST}}$ active edge, otherwise INL deteriorates. For example, if the clock frequency is 28 MHz, the clock must start within 71.4 ns of $\overline{\text{CONVST}}$ going low. In Figure 12, the A/D converter section is put into sleep mode once conversion is completed. On the rising edge of $\overline{\text{CONVST}}$, it is woken up again. The user must be wary of the wake-up time because it will reduce the sampling rate of the ADC.

V_{DRIVE}

The V_{DRIVE} pin is used as the voltage supply to the output drivers and is a separate supply from AV_{DD} and DV_{DD}. The purpose of using a separate supply for the output drivers is that the user can vary the output high voltage, V_{OH}, from the V_{DD} supply to the AD7470/AD7472. For example, if AV_{DD} and DV_{DD} is using a 5 V supply, the V_{DRIVE} pin can be powered from a 3 V supply. The ADC has better dynamic performance at 5 V than at 3 V, so operating the part at 5 V, while still being able to interface to 3 V parts, pushes the AD7470/AD7472 to the top bracket of high performance 10-bit/12-bit ADCs. Of course, the ADC can have its V_{DRIVE} and DV_{DD} pins connected together and be powered from a 3 V or 5 V supply.

All outputs are powered from V_{DRIVE}. These are all the data out pins and the BUSY pin. The $\overline{\text{CONVST}}$, $\overline{\text{CS}}$, $\overline{\text{RD}}$, and CLKIN signals are related to the DV_{DD} voltage.

POWER-UP

It is recommended that the user perform a dummy conversion after power-up, because the first conversion result could be incorrect. This also ensures that the part is in the correct mode of operation. The recommended power-up sequence is as follows:

1. GND
2. V_{DD}
3. V_{DRIVE}
4. Digital Inputs
5. REF IN
6. V_{IN}

Power vs. Throughput

The two modes of operation for the AD7470 and AD7472 will produce different power versus throughput performances, Mode 1 and Mode 2; see Operating Modes section of the data sheet for more detailed descriptions of these modes. Mode 2 is the sleep mode of the part and it achieves the optimum power performance.

Mode 1

Figure 14 shows the AD7472 conversion sequence in Mode 1 using a throughput rate of 500 kSPS and a clock frequency of 26 MHz. At 5 V supply, the current consumption for the part when converting is typically 2 mA, and the quiescent current is typically 650 µA. The conversion time of 531.66 ns contributes 2.658 mW to the overall power dissipation in the following way:

$$(531.66\ ns/2\ \mu s) \times (5 \times 2\ mA) = 2.658\ mW$$

The contribution to the total power dissipated by the remaining 1.468 µs of the cycle is 2.38 mW.

$$(1.468\ \mu s/2\ \mu s) \times (5 \times 650\ \mu A) = 2.38\ mW$$

Thus the power dissipated during each cycle is

$$2.658\ mW + 2.38\ mW = 5.038\ mW$$

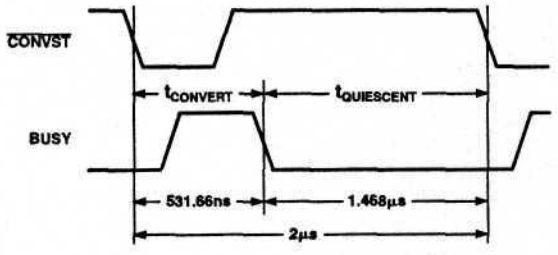


Figure 14. Mode 1 Power Dissipation

Mode 2

Figure 15 shows the AD7472 conversion sequence in Mode 2 using a throughput rate of 500 kSPS and a clock frequency of 26 MHz. At 5 V supply, the current consumption for the part when converting is typically 2 mA, while the sleep current is 1 µA max. The power dissipated during this power-down is negligible, and is thus not worth considering in the total power figure. During the wake-up phase, the AD7472 will draw 650 µA typically. Overall power dissipated is

$$(531.66\ ns / 2\ \mu s) \times (5 \times 2\ mA) + (1\ \mu s / 2\ \mu s) \times (5 \times 650\ \mu A) = 4.283\ mW$$

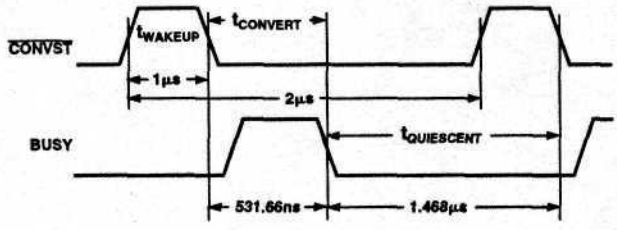


Figure 15. Mode 2 Power Dissipation

TPC 1 sand TPC 2 show a typical graphical representation of Power vs. Throughput for the AD7472 when in (a) Mode 1 @ 5 V and 3 V and Mode 2 @ 5 V and 3 V

National Semiconductor

July 2000

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample-and-Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

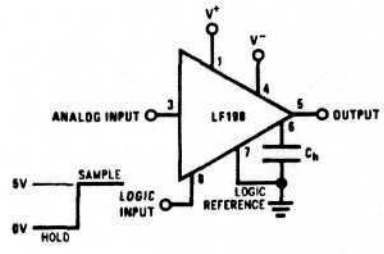
Features

- Operates from ±5V to ±18V supplies
- Less than 10 μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 μF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified, JM38510

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

An "A" version is available with tightened electrical specifications.

Typical Connection and Performance Curve



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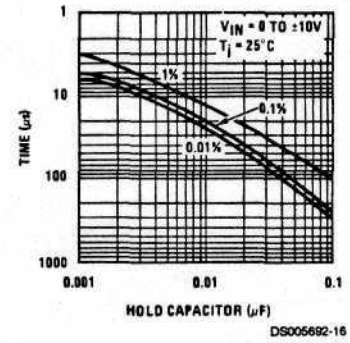
Acquisition Time



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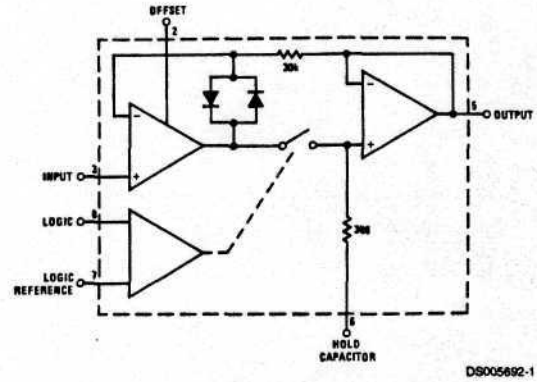
Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation (Package Limitation) (Note 2)	500 mW
Operating Ambient Temperature Range	
LF198/LF198A	−55°C to +125°C
LF298	−25°C to +85°C
LF398/LF398A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic To Logic Reference Differential Voltage (Note 3)	+7V, −30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10 sec
Lead Temperature (Note 4)	
H package (Soldering, 10 sec.)	260°C
N package (Soldering, 10 sec.)	260°C
M package:	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Thermal Resistance (θ_{JA}) (typicals)

H package 215°C/W (Board mount in still air)
85°C/W (Board mount in 400LF/min air flow)
N package 115°C/W
M package 106°C/W

θ_{JC} (H package, typical) 20°C/W

Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198/LF298			LF398			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage, (Note 5)	$T_j = 25°C$		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 5)	$T_j = 25°C$		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		80	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 6)	$T_j = 25°C$, $C_h = 0.01\ \mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 5)	$T_j \ge 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 5)	$T_j = 25°C$, (Note 7) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4			4		μs
	$C_h = 0.01\ \mu F$		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V
Input Offset Voltage, (Note 5)	$T_j = 25°C$		1	1		2	2	mV
	Full Temperature Range			2			3	mV
Input Bias Current, (Note 5)	$T_j = 25°C$		5	25		10	25	nA
	Full Temperature Range			75			50	nA

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Electrical Characteristics

The following specifcations apply for $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$, $+V_S = +15V$, $-V_S = -15V$, $T_A = T_j = 25°C$, $C_h = 0.01\ \mu F$, $R_L = 10\ k\Omega$, LOGIC REFERENCE = 0V, LOGIC HIGH = 2.5V, LOGIC LOW = 0V unless otherwise specified.

Parameter	Conditions	LF198A			LF398A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain Error	$T_j = 25°C$, $R_L = 10k$		0.002	0.005		0.004	0.005	%
	Full Temperature Range			0.01			0.01	%
Feedthrough Attenuation Ratio at 1 kHz	$T_j = 25°C$, $C_h = 0.01\ \mu F$	86	96		86	90		dB
Output Impedance	$T_j = 25°C$, "HOLD" mode		0.5	1		0.5	1	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 6)	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	1		1.0	1	mV
Supply Current, (Note 5)	$T_j \ge 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	$T_j = 25°C$		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 5)	$T_j = 25°C$, (Note 7) Hold Mode		30	100		30	100	pA
Acquisition Time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000$ pF		4	6		4	6	μs
	$C_h = 0.01\ \mu F$		20	25		20	25	μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply Voltage Rejection Ratio	$V_{OUT} = 0$	90	110		90	110		dB
Differential Logic Threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$, or the number given in the Absolute Maximum Ratings, whichever is lower. The maximum junction temperature, T_{JMAX}, for the LF198/LF198A is 150°C; for the LF298, 115°C; and for the LF398/LF398A, 100°C.

Note 3: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 4: See AN-450 "Surface Mounting Methods and their effects on Product Reliability" for other methods of soldering surface mount devices.

Note 5: These parameters guaranteed over a supply voltage range of ±5 to ±18V, and an input range of $-V_S + 3.5V \le V_{IN} \le +V_S - 3.5V$.

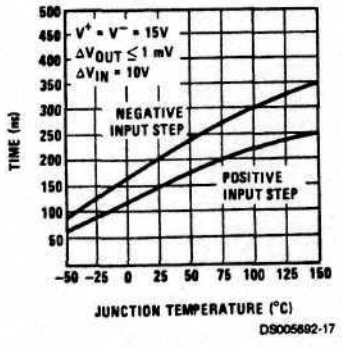
Note 6: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 7: Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

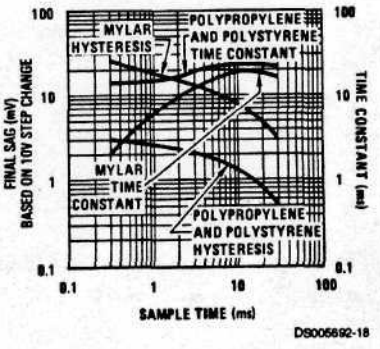
Note 8: A military RETS electrical test specification is available on request. The LF198 may also be procured to Standard Military Drawing #5962-8760801GA or to MIL-STD-38510 part ID JM38510/12501SGA.

Typical Performance Characteristics

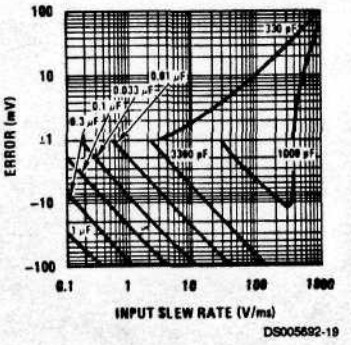
Aperture Time
(Note 9)



Dielectric Absorption Error in Hold Capacitor



Dynamic Sampling Error



Note 9: See Definition of Terms

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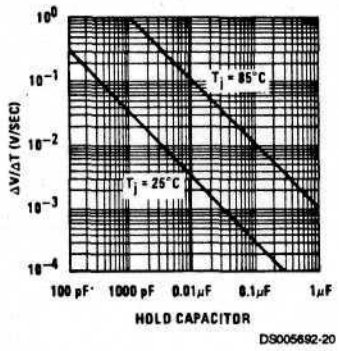
Typical Performance Characteristics (Continued)

Output Droop Rate



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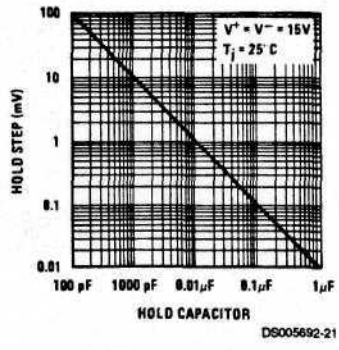
Hold Step



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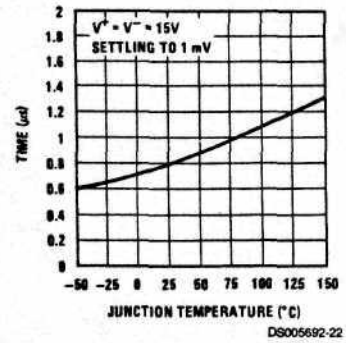
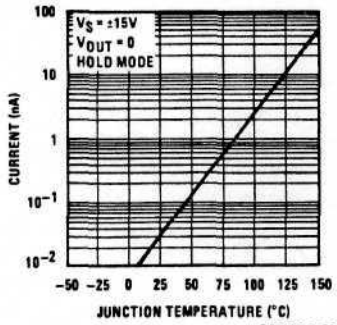
"Hold" Settling Time
(Note 10)



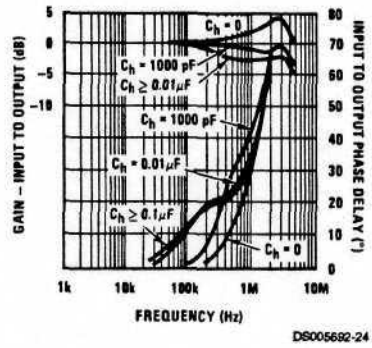
DS005692-22

Leakage Current into Hold Capacitor



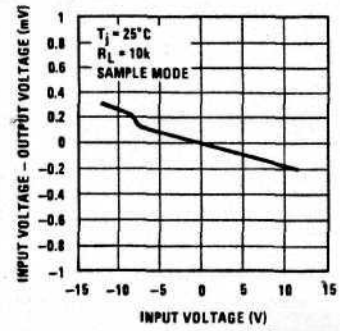
DS005692-23

Phase and Gain (Input to Output, Small Signal)



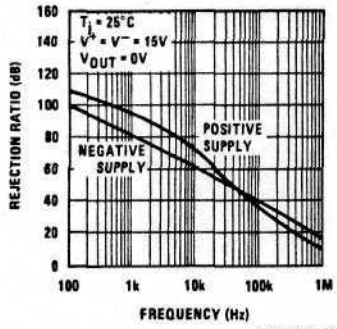
DS005692-24

Gain Error



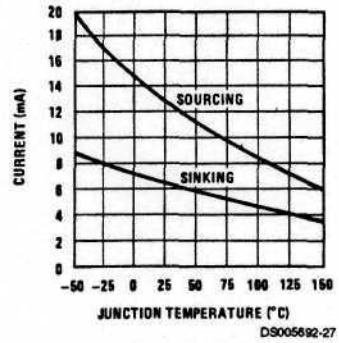
DS005692-25

Power Supply Rejection



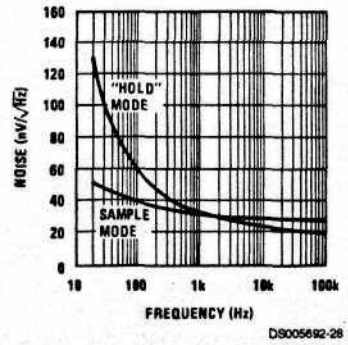
DS005692-26

Output Short Circuit Current



DS005692-27

Output Noise



DS005692-28

Note 10: See Definition

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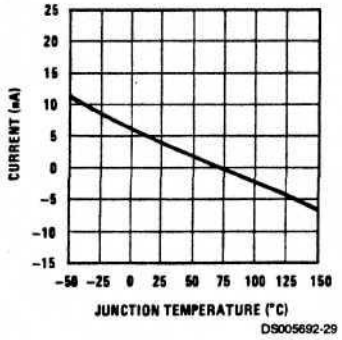
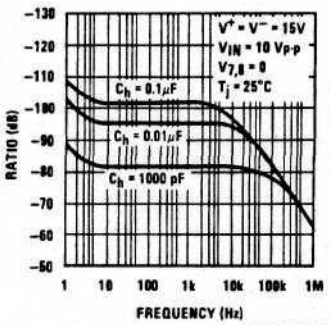
Typical Performance Characteristics (Continued)

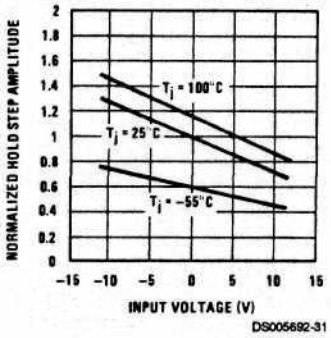
Input Bias Current



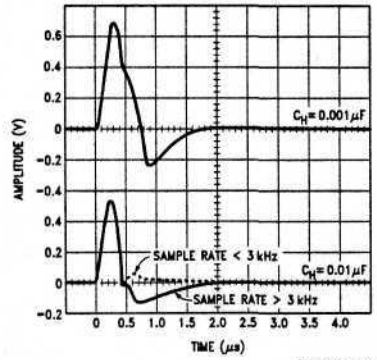
Feedthrough Rejection Ratio (Hold Mode)



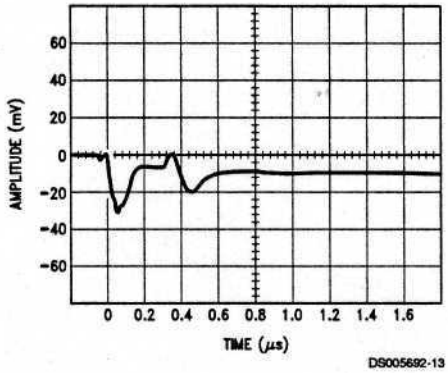
Hold Step vs Input Voltage



Output Transient at Start of Sample Mode

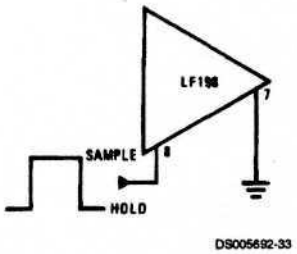


Output Transient at Start of Hold Mode

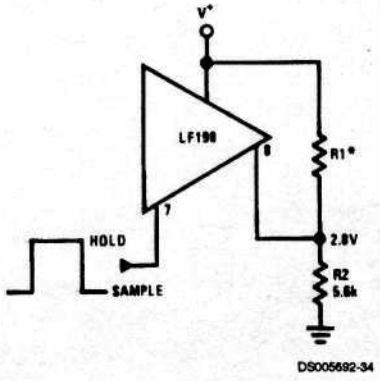


Logic Input Configurations

TTL & CMOS
$3V \leq V_{LOGIC}$ (Hi State) $\leq 7V$



Threshold = 1.4V



Threshold = 1.4V
*Select for 2.8V at pin 8

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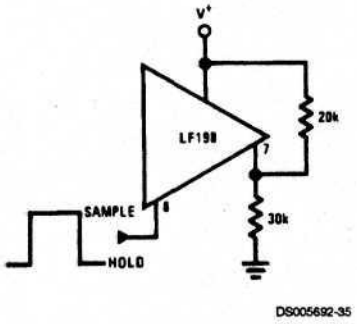
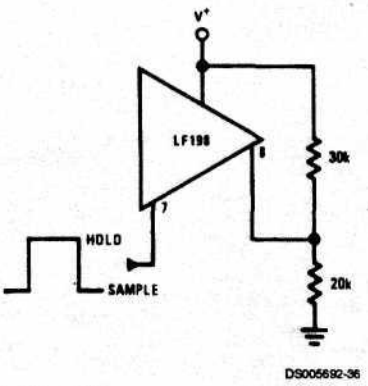
Logic Input Configurations (Continued)

CMOS

$7V \leq V_{LOGIC}$ (Hi State) $\leq 15V$

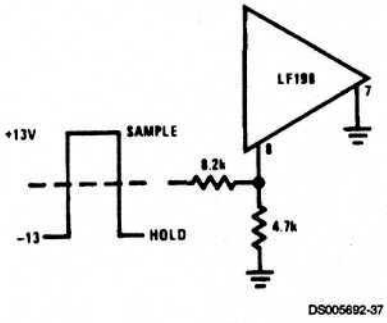


Threshold = 0.6 (V^+) + 1.4V

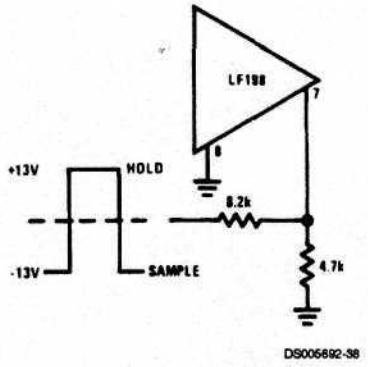


Threshold = 0.6 (V^+) − 1.4V

Op Amp Drive



Threshold ≈ +4V



Threshold = −4V

Application Hints

Hold Capacitor

Hold step, acquisition time, and droop rate are the major trade-offs in the selection of a hold capacitor value. Size and cost may also become important for larger values. Use of the curves included with this data sheet should be helpful in selecting a reasonable value of capacitance. Keep in mind that for fast repetition rates or tracking fast signals, the capacitor drive currents may cause a significant temperature rise in the LF198.

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long sample time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. Most ceramic capacitors are unusable with > 1% hysteresis. Ceramic "NPO" or "COG" capacitors are now available for 125°C operation and also have low dielectric absorption. For more exact data, see the curve *Dielectric Absorption Error*. The hysteresis numbers on the curve are final values, taken after full relaxation. The hysteresis error can be significantly reduced if the output of the LF198 is digitized quickly after the hold mode is initiated. The hysteresis relaxation time constant in polypropylene, for instance, is 10—50 ms. If A-to-D conversion can be made within 1 ms, hysteresis error will be reduced by a factor of ten.

DC and AC Zeroing

DC zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1 kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≈0.6 mA through the 1k potentiometer.

AC zeroing (hold step zeroing) can be obtained by adding an inverter with the adjustment pot tied input to output. A 10 pF capacitor from the wiper to the hold capacitor will give ±4 mV hold step adjustment with a 0.01 μF hold capacitor and 5V logic supply. For larger logic swings, a smaller capacitor (< 10 pF) may be used.

Logic Rise Time

For proper operation, logic signals into the LF198 must have a minimum dV/dt of 1.0 V/μs. Slower signals will cause excessive hold step. If a R/C network is used in front of the

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Application Hints (Continued)

logic input for signal delay, calculate the slope of the waveform at the threshold point to ensure that it is at least 1.0 V/μs.

Sampling Dynamic Signals

Sample error to moving input signals probably causes more confusion among sample-and-hold users than any other parameter. The primary reason for this is that many users make the assumption that the sample and hold amplifier is truly locked on to the input signal while in the sample mode. In actuality, there are finite phase delays through the circuit creating an input-output differential for fast moving signals. In addition, although the output may have settled, the hold capacitor has an additional lag due to the 300Ω series resistor on the chip. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10 kHz. Maximum dV/dt is 0.6 V/μs. With no analog phase delay and 100 ns logic delay, one could expect up to (0.1 μs) (0.6V/μs) = 60 mVerror if the "hold" signal arrived near maximum dV/dt of the input. A positive-going input would give a +60 mV error. Now assume a 1 MHz (3 dB) bandwidth for the overall analog loop. This generates a phase delay of 160 ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16 μs) (0.6 V/μs) = −96 mV. Total output error is +60 mV (digital) −96 mV (analog) for a total of −36 mV. To add to the confusion, analog delay is proportioned to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

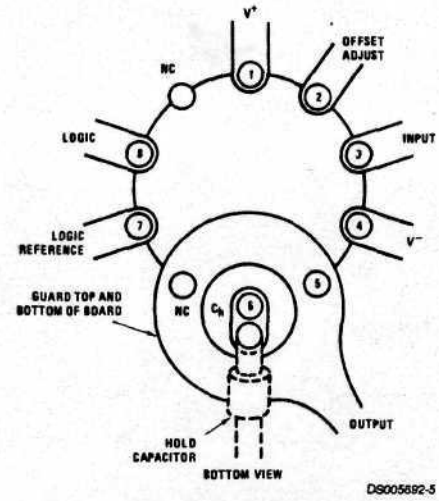
A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1 mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1 mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input and the C_h pin. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Guarding Technique



Use 10-pin layout. Guard around C_h is tied to output.

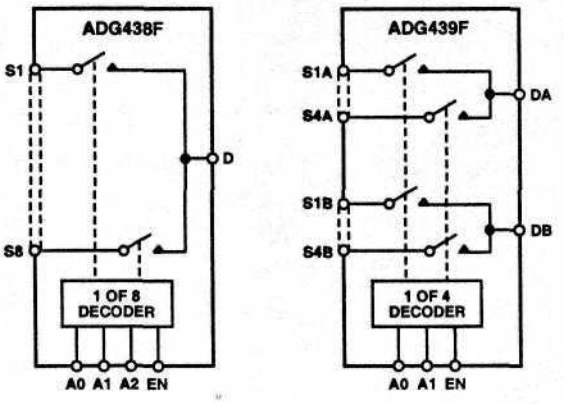
High Performance 4/8 Channel Fault-Protected Analog Multiplexers

ADG438F/ADG439F*

FEATURES
- Fast Switching Times
  - t_{ON} 250 ns max
  - t_{OFF} 150 ns max
- Fault and Overvoltage Protection (–40 V, +55 V)
- All Switches OFF with Power Supply OFF
- Analog Output of ON Channel Clamped Within Power Supplies If an Overvoltage Occurs
- Latch-Up Proof Construction
- Break Before Make Construction
- TTL and CMOS Compatible Inputs

APPLICATIONS
- Data Acquisition Systems
- Industrial and Process Control Systems
- Avionics Test Equipment
- Signal Routing Between Systems
- High Reliability Control Systems

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG438F/ADG439F are CMOS analog multiplexers, the ADG438F comprising 8 single channels and the ADG439F comprising four differential channels. These multiplexers provide fault protection. Using a series n-channel, p-channel, n-channel MOSFET structure, both device and signal source protection is provided in the event of an overvoltage or power loss. The multiplexer can withstand continuous overvoltage inputs from –40 V to +55 V. During fault conditions, the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry driven by the multiplexer, but also protects the sensors or signal sources which drive the multiplexer.

The ADG438F switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG439F switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on each device is used to enable or disable the device. When disabled, all channels are switched OFF.

PRODUCT HIGHLIGHTS

1. Fault Protection.
   The ADG438F/ADG439F can withstand continuous voltage inputs up to –40 V or +55 V. When a fault occurs due to the power supplies being turned off, all the channels are turned off and only a leakage current of a few nanoamperes flows.
2. ON channel turns OFF while fault exists.
3. Low R_{ON}.
4. Fast Switching Times.
5. Break-Before-Make Switching.
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Trench Isolation Eliminates Latch-up.
   A dielectric trench separates the p- and n-channel MOSFETs thereby preventing latch-up.
7. Improved OFF Isolation.
   Trench isolation enhances the channel-to-channel isolation of the ADG438F/ADG439F.

*Patent Pending.

REV. D

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Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADG438F/ADG439F–SPECIFICATIONS[1]

Dual Supply (V_{DD} = +15 V, V_{SS} = –15 V, GND = 0 V, unless otherwise noted)

Parameter	+25°C	B Version –40°C to +85°C	–40°C to +105°C	Units	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range		V_{SS} + 1.2	V_{SS} + 1.2	V min	
		V_{DD} – 0.8	V_{DD} – 0.8	V max	
R_{ON}		400	400	Ω max	–10 V ≤ V_S ≤ +10 V, I_S = 1 mA;
ΔR_{ON}		5	5	% max	–5 V ≤ V_S ≤ +5 V, I_S = 1 mA;
R_{ON} Drift	0.6			%/°C typ	V_S = 0 V, I_S = 1 mA
R_{ON} Match	3	3	3	% max	V_S = ±10 V, I_S = 1 mA
LEAKAGE CURRENTS					
Source OFF Leakage I_S (OFF)	±0.01			nA typ	V_D = ±10 V, V_S = ∓10 V;
	±0.5	±2	±5	nA max	Test Circuit 2
Drain OFF Leakage I_D (OFF)	±0.01			nA typ	V_D = ±10 V, V_S = ∓10 V;
ADG438F	±0.5	±5	±30	nA max	Test Circuit 3
ADG439F	±0.5	±5	±15	nA max	
Channel ON Leakage I_D, I_S (ON)	±0.01			nA typ	V_S = V_D = ±10 V;
ADG438F	±0.5	±5	±30	nA max	Test Circuit 4
ADG439F	±0.5	±5	±15	nA max	
FAULT					
Output Leakage Current	±0.02			nA typ	V_S = –33 V, +33 V or +50 V, V_D = 0 V, Test Circuit 3
(With Overvoltage)	±0.1	±2	±10	μA max	
Input Leakage Current	±0.005			μA typ	V_S = ±25 V, V_D = ∓10 V, Test Circuit 5
(With Overvoltage)	±0.1	±1	±2	μA max	
Input Leakage Current	±0.001			μA typ	V_S = ±25 V, V_D = V_{EN} = A0, A1, A2 = 0 V
(With Power Supplies OFF)	±0.1	±1	±4	μA max	Test Circuit 6
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2.4	2.4	V min	
Input Low Voltage, V_{INL}		0.8	0.8	V max	
Input Current					
I_{INL} or I_{INH}		±1	±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
$t_{TRANSITION}$	170			ns typ	R_L = 1 MΩ, C_L = 35 pF;
	220	300	320	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; Test Circuit 7
t_{OPEN}	10	10	10	ns min	R_L = 1 kΩ, C_L = 35 pF;
					V_S = +5 V; Test Circuit 8
t_{ON} (EN)	200			ns typ	R_L = 1 kΩ, C_L = 35 pF;
	250	300	300	ns max	V_S = +5 V; Test Circuit 9
t_{OFF} (EN)	110			ns typ	R_L = 1 kΩ, C_L = 35 pF;
	150	180	180	ns max	V_S = +5 V; Test Circuit 9
t_{SETT}, Settling Time					
0.1%		0.5	0.5	μs typ	R_L = 1 kΩ, C_L = 35 pF;
0.01%		1.7	1.7	μs typ	V_S = +5 V
Charge Injection	4			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 10
OFF Isolation	80			dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
					V_S = 7 V rms; Test Circuit 11
Channel-to-Channel Crosstalk	85			dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz;
					V_S = 7 V rms; Test Circuit 12
C_S (OFF)	5			pF typ	
C_D (OFF)					
ADG438F	50			pF typ	
ADG439F	25			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.05			mA typ	V_{IN} = 0 V or 5 V
	0.15	0.25	0.25	mA max	
I_{SS}	0.01			mA typ	
	0.02	0.04	0.04	mA max	

NOTES
[1]Temperature range is as follows: B Version: –40°C to +105°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

REV. D

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ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} ..... +44 V
V_{DD} to GND ..... –0.3 V to +25 V
V_{SS} to GND ..... +0.3 V to –25 V
V_{EN}, V_A Digital Input ..... – 0.3 V to V_{DD} + 2 V or 20 mA, Whichever Occurs First
V_S, Analog Input Overvoltage with Power ON ..... V_{SS} – 25 V to V_{DD} + 40 V
V_S, Analog Input Overvoltage with Power OFF ..... –40 V to +55 V
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle max) ..... 40 mA
Operating Temperature Range
Industrial (B Version) ..... –40°C to +105°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
Plastic Package
θ_{JA}, Thermal Impedance ..... 117°C/W
Lead Temperature, Soldering (10 sec) ..... +260°C
SOIC Package
θ_{JA}, Thermal Impedance
Narrow Body ..... 125°C/W
Wide Body ..... 90°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG438FBN	–40°C to +105°C	N-16
ADG438FBR	–40°C to +105°C	R-16N
ADG439FBN	–40°C to +105°C	N-16
ADG439FBR	–40°C to +105°C	R-16N
ADG439FBRW	–40°C to +105°C	R-16W

*N = Plastic DIP; R-16N = 0.15" Small Outline IC (SOIC); R-16W = 0.3" Small Outline IC (SOIC).

Table I. ADG438F Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

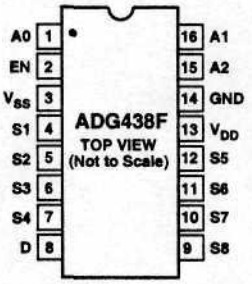
Table II. ADG439F Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

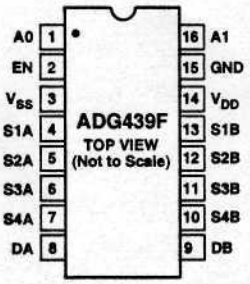
X = Don't Care

ADG438F/ADG439F PIN CONFIGURATIONS

DIP/SOIC



DIP/SOIC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG438F/ADG439F features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	R_{ON} variation due to a change in the analog input voltage with a constant load current.
R_{ON} Drift	Change in R_{ON} when temperature changes by one degree Celsius.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for Logic "0".
V_{INH}	Minimum input voltage for Logic "1".
I_{INL} (I_{INH})	Input current of the digital input.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

Typical Performance Graphs

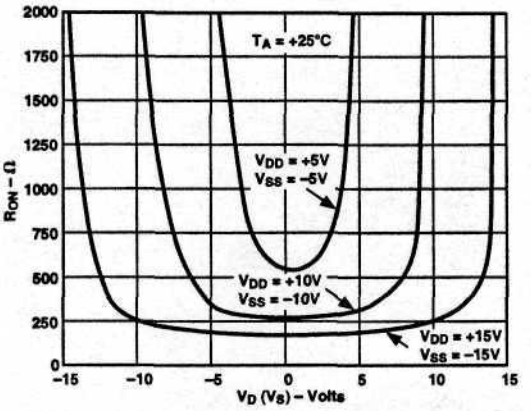


Figure 1. On Resistance as a Function of V_D (V_S)

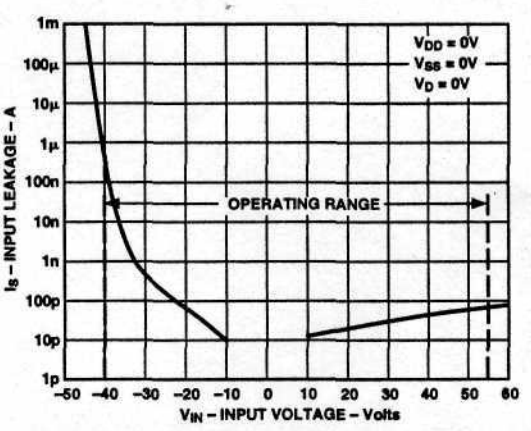


Figure 2. Input Leakage Current as a Function of V_S (Power Supplies OFF) During Overvoltage Conditions

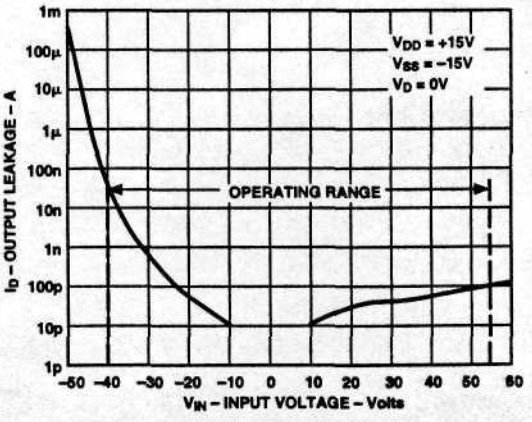


Figure 3. Output Leakage Current as a Function of V_S (Power Supplies ON) During Overvoltage Conditions

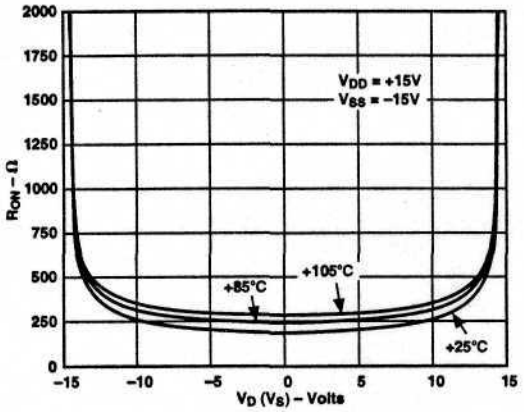


Figure 4. On Resistance as a Function of V_D (V_S) for Different Temperatures

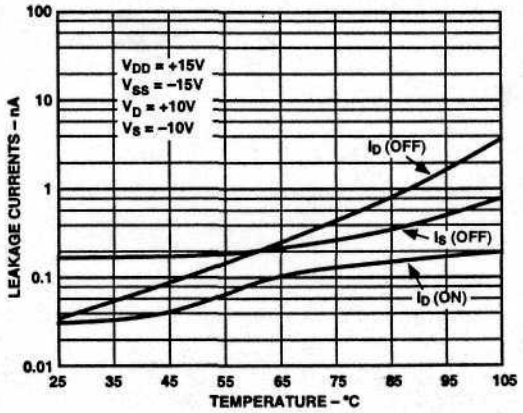


Figure 7. Leakage Currents as a Function of Temperature

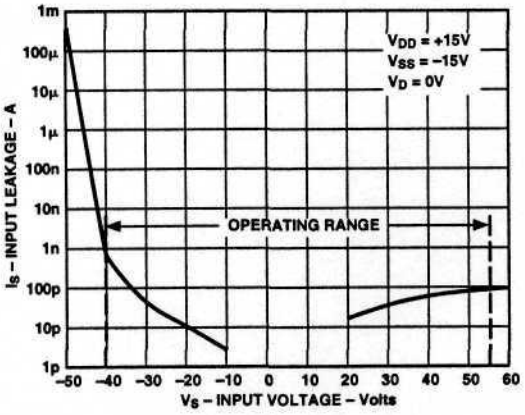


Figure 5. Input Leakage Current as a Function of V_S (Power Supplies ON) During Overvoltage Conditions

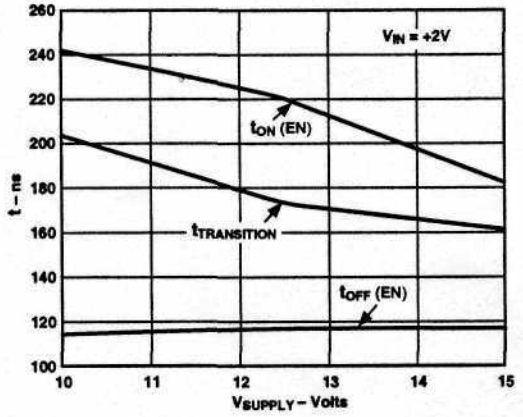


Figure 8. Switching Time vs. Power Supply

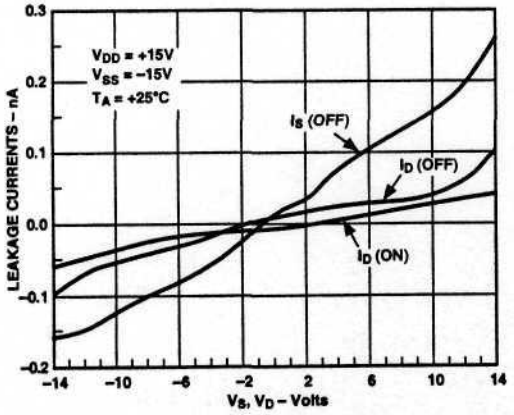


Figure 6. Leakage Currents as a Function of V_D (V_S)

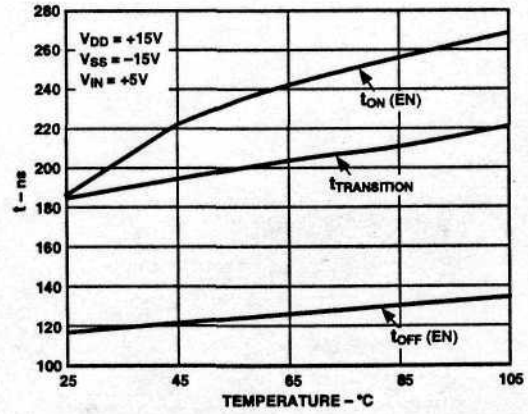


Figure 9. Switching Time vs. Temperature

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