ESAMI DI STATO PER L'ABILITAZIONE ALLA PROFESSIONE DI INGEGNERE

VECCHIO ORDINAMENTO - II SESSIONE 2009

Ramo Elettronica

Tema n. 1

Il candidato progetti un misuratore di energia elettrica (contatore elettrico), operante in regime alternato con frequenza di rete pari a 50 Hz, da installare in case di civile abilitazione con contratto di potenza massima erogata pari a 3 kW.

Il contatore dovra' essere realizzato utilizzando i moderni dispositivi elettronici (convertitori A/D, DSP), di cui esempi sono dati negli allegati.

Il contatore dovra' soddisfare le seguenti principali specifiche:

- Accettare un valore efficace della tensione in ingresso variabile fra 200V e 280 V
- Accettare un valore efficace della corrente in ingresso variabile fra 0 A e 25 A
- Accettare un coseno dell'angolo di fase fra tensione e corrente di valore qualunque fra 0 e 1.
- Fornire la misura con incertezza relativa uguale o inferiore a 0,1%, stimata nelle seguenti condizioni operative:
  - Valore efficace della corrente pari a 16 A
  - Valore efficace della tensione pari a 220 V
  - Coseno angolo di fase pari ad 1
  - Segnali in ingresso: sinusoidali con frequenza pari a 50 Hz
  - Intervallo di osservazione: 3600 s
- Misurare l'energia erogata fino alla decima armonica rispetto alla sinusoide fondamentale alla frequenza di 50 Hz

Il contatore dovra':

- Fornire in uscita, su linea seriale, il valore dell'energia consumata in un intervallo di tempo prestabilito (tipicamente fra l'istante di

installazione/avviamento dell'apparecchiatura e quello di lettura) e della potenza istantanea assorbita

- Emulare un interruttore magnetotermico, comandando in apertura un interruttore di linea nel caso in cui la corrente erogata superi il 10% del valore massimo contrattuale per piu' di tre ore ed entro 200 ms nel caso di valori superiori di corrente
- Fornire su un display locale l'informazione dell'energia consumata, della potenza massima istantanea e storica (valore riportabile a zero dall'utente) assorbita, del massimo valore storico dell'angolo di fase (valore riportabile a zero dall'utente) e di indicazioni di allarme per il superamento delle soglie contrattuali.

Si chiede al candidato di:

1. Definire lo schema a blocchi dell'intero strumento, indicando per ciascun blocco le specifiche funzionalità che esso deve svolgere e le connessioni con gli altri blocchi;
2. Per ciascun blocco individuare il tipo di realizzazione ritenuta più adatta al progetto dando indicazioni sui componenti che si ha intenzione di utilizzare (caratteristiche principali, se possibile la sigla commerciale e le informazioni per poter reperire la pagina del manuale di riferimento, cartaceo o in rete internet)
3. Progettare almeno uno dei blocchi individuati a livello di schema elettrico.
4. Indicare lo schema di flusso del *software* di programmazione necessario, in modo che sia strutturato nei principali procedimenti *software* che realizzano le varie funzionalita'

Facoltativo: di un procedimento software presentare il diagramma di flusso dettagliato, a un livello tale da permettere l'immediata scrittura del codice sorgente in un linguaggio ad alto livello

Discutere infine:

- Le principali criticità del sistema;
- Le principali cause di incertezza che concorrono a determinare quella globale dello strumento, della quale si chiede di fornire una stima (eventualmente anche in condizioni differenti da quelle indicate precedentemente in sede di dichiarazione delle specifiche)

16-Bit, 4-Channel/8-Channel, 250 kSPS PulSAR ADC

AD7682/AD7689

FEATURES

- 16-bit resolution with no missing codes
- 4-channel (AD7682)/8-channel (AD7689) multiplexer with choice of inputs
  - Unipolar single-ended
  - Differential (GND sense)
  - Pseudobipolar
- Throughput: 250 kSPS
- INL: ±0.4 LSB typical, ±1.5 LSB maximum (±23 ppm or FSR)
- Dynamic range: 93.8 dB
- SINAD: 92.5 dB @ 20 kHz
- THD: −100 dB @ 20 kHz
- Analog input range: 0 V to V_{REF} with V_{REF} up to VDD
- Multiple reference types
  - Internal selectable 2.5 V or 4.096 V
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor (TEMP)
- Channel sequencer, selectable 1-pole filter, busy indicator
- No pipeline delay, SAR architecture
- Single-supply 2.3 V to 5.5 V operation with 1.8 V to 5.5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP
- Power dissipation
  - 3.5 mW @ 2.5 V/200 kSPS
  - 12.5 mW @ 5 V/250 kSPS
- Standby current: 50 nA
- Low cost grade available
- 20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

- Multichannel system monitoring
- Battery-powered equipment
- Medical instruments: ECG/EKG
- Mobile communications: GPS
- Power line monitoring
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process control

FUNCTIONAL BLOCK DIAGRAM

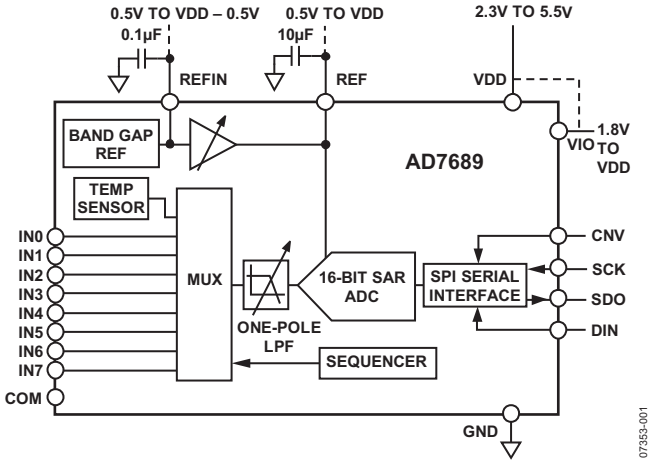

Figure 1.

Table 1. Multichannel 14-/16-Bit PulSAR® ADC

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4841-x
16-Bit	4	AD7682		ADA4841-x
16-Bit	8	AD7689	AD7699	ADA4841-x

GENERAL DESCRIPTION

The AD7682/AD7689 are 4-channel/8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converters (ADCs) that operate from a single power supply, VDD.

The AD7682/AD7689 contain all components for use in a multichannel, low power data acquisition system, including a true 16-bit SAR ADC with no missing codes; a 4-channel (AD7682) or 8-channel (AD7689), low crosstalk multiplexer that is useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal low drift reference (selectable 2.5 V or 4.096 V) and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The AD7682/AD7689 use a simple SPI interface for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The AD7682/AD7689 are housed in a tiny 20-lead LFCSP with operation specified from −40°C to +85°C.

Rev. A

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SPECIFICATIONS

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

		AD7689A			AD7682B/AD7689B			
Parameter	**Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range	Unipolar mode	0		$+V_{REF}$	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	$-V_{REF}/2$		$+V_{REF}/2$	
Absolute Input Voltage	Positive input, unipolar and bipolar modes	−0.1		V_{REF} + 0.1	−0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	−0.1		+0.1	−0.1		+0.1	V
	Negative or COM input, bipolar mode	$V_{REF}/2$ − 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	$V_{REF}/2$ − 0.1	$V_{REF}/2$	$V_{REF}/2$ + 0.1	V
Analog Input CMRR	f_{IN} = 250 kHz		68			68		dB
Leakage Current at 25°C	Acquisition phase		1			1		nA
Input Impedance[1]								
THROUGHPUT								
Conversion Rate								
Full Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		250	0		250	kSPS
	VDD = 2.3 V to 4.5 V	0		200	0		200	kSPS
¼ Bandwidth[2]	VDD = 4.5 V to 5.5 V	0		62.5	0		62.5	kSPS
	VDD = 2.3 V to 4.5 V	0		50	0		50	kSPS
Transient Response	Full-scale step, full bandwidth			1.8			1.8	µs
	Full-scale step, ¼ bandwidth			14.5			14.5	µs
ACCURACY								
No Missing Codes		15			16			Bits
Integral Linearity Error		−4		+4	−1.5	±0.4	+1.5	LSB[3]
Differential Linearity Error					−1	±0.25	+1.5	LSB
Transition Noise	REF = VDD = 5 V		0.6			0.5		LSB
Gain Error[4]		−32		+32	−8	±1	+8	LSB
Gain Error Match			±2		−4	±0.5	+4	LSB
Gain Error Temperature Drift			±1			±1		ppm/°C
Offset Error[4]	VDD = 4.5 V to 5.5 V	−32		+32	−8	±1	+8	LSB
	VDD = 2.3 V to 4.5 V		±32			±5		LSB
Offset Error Match			±2		−4	±0.5	+4	LSB
Offset Error Temperature Drift			±1			±1		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±1.5			±1.5		LSB
AC ACCURACY[5]								
Dynamic Range			90.5			93.8		dB[6]
Signal-to-Noise	f_{IN} = 20 kHz, V_{REF} = 5 V		90		92.5	93.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V, internal REF		89		91	92.3		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V, internal REF		86		87.5	88.8		dB
SINAD	f_{IN} = 20 kHz, V_{REF} = 5 V		89		91	92.5		dB
	f_{IN} = 20 kHz, V_{REF} = 5 V, −60 dB input		30.5			33.5		dB
	f_{IN} = 20 kHz, V_{REF} = 4.096 V internal REF		88		90	91		dB
	f_{IN} = 20 kHz, V_{REF} = 2.5 V internal REF		86		87	88.4		dB

VDD = 2.3 V to 5.5 V, VIO = 1.8 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Conditions/Comments	All Models/Grades Min	Typ	Max	Unit
INTERNAL REFERENCE					
REF Output Voltage	2.5 V, @ 25°C	2.490	2.500	2.510	V
	4.096 V, @ 25°C	4.086	4.096	4.106	V
REFIN Output Voltage[1]	2.5 V, @ 25°C		1.2		V
	4.096 V, @ 25°C		2.3		V
REF Output Current			±300		µA
Temperature Drift			±10		ppm/°C
Line Regulation	VDD = 5 V ± 5%		±15		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	C_{REF} = 10 µF		5		ms
EXTERNAL REFERENCE					
Voltage Range	REF input	0.5		VDD + 0.3	V
	REFIN input (buffered)	0.5		VDD − 0.5	V
Current Drain[2]	250 kSPS, REF = 5 V		50		µA
TEMPERATURE SENSOR					
Output Voltage[3]	@ 25°C		283		mV
Temperature Sensitivity			1		mV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[4]					
Pipeline Delay[5]					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	2.3		5.5	V
VIO	Specified performance	1.8		VDD + 0.3	V
Standby Current[6, 7]	VDD and VIO = 5 V, @ 25°C		50		nA
Power Dissipation	VDD = 2.5 V, 100 SPS throughput		1.7		µW
	VDD = 2.5 V, 200 kSPS throughput		3.5		mW
	VDD = 5 V, 250 kSPS throughput		12.5	18	mW
	VDD = 5 V, 250 kSPS throughput with internal reference		15.5	21	mW
Energy per Conversion	VDD = 5V		60		nJ
TEMPERATURE RANGE[8]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] This is the output from the internal band gap.
[2] This is an average current and scales with throughput.
[3] The output voltage is internal and present on a dedicated multiplexer input.
[4] Unipolar mode: serial 16-bit straight binary.
Bipolar mode: serial 16-bit twos complement.
[5] Conversion results available immediately after completed conversion.
[6] With all digital inputs forced to VIO or GND as required.
[7] During acquisition phase.
[8] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

16-Bit, 8-Channel, 500 kSPS PulSAR ADC

AD7699

FEATURES

- 16-bit resolution with no missing codes
- 8-channel multiplexer with choice of inputs
  - Unipolar single-ended
  - Differential (GND sense)
  - Pseudobipolar
- Throughput: 500 kSPS
- INL: ±0.5 LSB typical, ±1.5 LSB maximum (±23 ppm or FSR)
- Dynamic range: 93.3 dB
- SINAD: 91.5 dB @ 20 kHz
- THD: −97 dB @ 20 kHz
- Analog input range: 0 V to V_{REF} with V_{REF} up to VDD
- Multiple reference types
  - Internal 4.096 V
  - External buffered (up to 4.096 V)
  - External (up to VDD)
- Internal temperature sensor
- Channel sequencer, selectable 1-pole filter, busy indicator
- No pipeline delay, SAR architecture
- Single-supply 5 V operation with
  - 1.8 V to 5 V logic interface
- Serial interface compatible with SPI, MICROWIRE, QSPI, and DSP
- Power dissipation
  - 26 mW @ 500 kSPS
  - 5.2 µW @ 100 SPS
- Standby current: 50 nA
- 20-lead 4 mm × 4 mm LFCSP package

APPLICATIONS

- Battery-powered equipment
- Medical instruments: ECG/EKG
- Mobile communications: GPS
- Personal digital assistants
- Power line monitoring
- Data acquisition
- Seismic data acquisition systems
- Instrumentation
- Process control

FUNCTIONAL BLOCK DIAGRAM

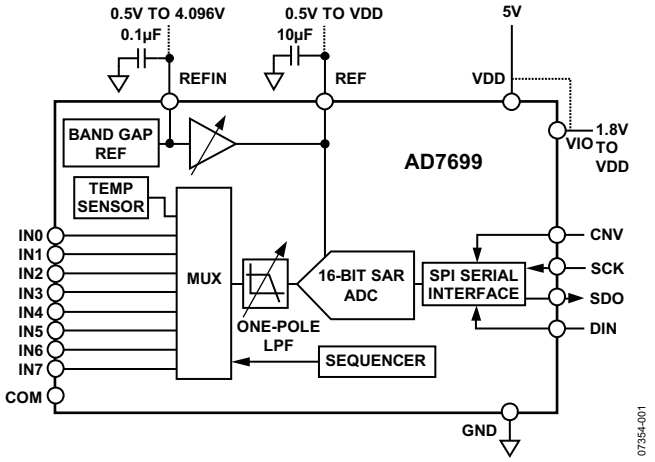

Figure 1.

Table 1. Multichannel 14-/16-Bit PulSAR® ADC

Type	Channels	250 kSPS	500 kSPS	ADC Driver
14-Bit	8	AD7949		ADA4841-x
16-Bit	4	AD7682		ADA4841-x
16-Bit	8	AD7689	AD7699	ADA4841-x

GENERAL DESCRIPTION

The AD7699 is an 8-channel, 16-bit, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) that operates from a single power supply, VDD.

The AD7699 contains all components for use in a multichannel, low power data acquisition system, including a true 16-bit SAR ADC with no missing codes; an 8-channel low crosstalk multiplexer useful for configuring the inputs as single-ended (with or without ground sense), differential, or bipolar; an internal 4.096 V low drift reference and buffer; a temperature sensor; a selectable one-pole filter; and a sequencer that is useful when channels are continuously scanned in order.

The AD7699 uses a simple serial port interface (SPI) for writing to the configuration register and receiving conversion results. The SPI interface uses a separate supply, VIO, which is set to the host logic level. Power dissipation scales with throughput.

The AD7699 is housed in a tiny 20-lead LFCSP with operation specified from −40°C to +85°C.

Rev. 0

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SPECIFICATIONS

VDD = 4.5 V to 5.5 V, V_{REF} = 4.096 to VDD, VIO = 1.8 V to VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	Unipolar mode	0		$+V_{REF}$	V
	Bipolar mode	$-V_{REF}/2$		$+V_{REF}/2$	V
Absolute Input Voltage	Positive input, unipolar and bipolar modes	−0.1		V_{REF} + 0.1	V
	Negative or COM input, unipolar mode	−0.1		+0.1	V
	Negative or COM input, bipolar mode	$V_{REF}/2 - 0.1$	$V_{REF}/2$	$V_{REF}/2 + 0.1$	V
Analog Input CMRR	f_{IN} = 250 kHz		68		dB
Leakage Current at 25°C Input Impedance[1]	Acquisition phase		1		nA
THROUGHPUT					
Conversion Rate					
Full Bandwidth[2]		0		500	kSPS
¼ Bandwidth[2]		0		125	kSPS
Transient Response	Full-scale step, full bandwidth			400	ns
	Full-scale step, ¼ bandwidth			1600	ns
ACCURACY					
No Missing Codes		16			Bits
Integral Linearity Error		−1.5	±0.5	+1.5	LSB[3]
Differential Linearity Error		−1	±0.25	+1.5	LSB
Transition Noise	REF = VDD = 5 V		0.5		LSB
Gain Error[4]	All modes	−10	±1	+10	LSB
Gain Error Match		−3	±1	+3	LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Offset Error[4]	All modes	−10	±1	+10	LSB
Offset Error Match		−3	±1	+3	LSB
Offset Error Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±1.5		LSB
AC Accuracy					
Dynamic Range			93.3		dB[5]
Signal-to-Noise	f_{IN} = 20 kHz, VREF = 5 V	92	92.5		dB
	f_{IN} = 20 kHz, VREF = 4.096 V internal REF	89.5	91.5		dB
SINAD	f_{IN} = 20 kHz, VREF = 5 V	90	91.5		dB
	f_{IN} = 20 kHz, VREF = 5 V, −60 dB input		33.5		dB
	f_{IN} = 20 kHz, VREF = 4.096 V internal REF	89	90.5		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		−97		dB
Spurious-Free Dynamic Range	f_{IN} = 20 kHz		112		dB
Channel-to-Channel Crosstalk	f_{IN} = 100 kHz on adjacent channel(s)		−125		dB
SAMPLING DYNAMICS					
−3 dB Input Bandwidth	Full bandwidth		14		MHz
	¼ bandwidth		3.6		MHz
Aperture Delay	VDD = 5 V		2.5		ns

Parameter	Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE					
REF Output Voltage	@ 25°C	4.086	4.096	4.106	V
REFIN Output Voltage[6]	@ 25°C		2.3		V
REF Output Current			±300		µA
Temperature Drift			±10		ppm/°C
Line Regulation	VDD = 5 V ± 5%		±15		ppm/V
Long-Term Drift	1000 hours		50		ppm
Turn-On Settling Time	CREF = 10 µF		5		ms
EXTERNAL REFERENCE					
Voltage Range	REF input	0.5		VDD + 0.3	V
	REFIN input (buffered)	0.5		VDD − 0.2	V
Current Drain	500 kSPS, REF = 5 V		100		µA
TEMPERATURE SENSOR					
Output Voltage[7]	@ 25°C		283		mV
Temperature Sensitivity			1		mV/°C
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format[8]					
Pipeline Delay[9]					
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	4.5		5.5	V
VIO	Specified performance	1.8		VDD + 0.3	V
Standby Current[10, 11]	VDD and VIO = 5 V, @ 25°C		50		nA
Power Dissipation	VDD = 5 V, 100 kSPS throughput		5.2		µW
	VDD = 5 V, 500 kSPS throughput		26	29	mW
	VDD = 5 V, 500 kSPS throughput with internal reference		28	32	mW
Energy per Conversion			52		nJ
TEMPERATURE RANGE[12]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] See the Analog Inputs section.
[2] The bandwidth is set with the configuration register.
[3] LSB means least significant bit. With the 5 V input range, one LSB = 76.3 µV.
[4] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the reference.
[5] All specifications expressed in decibels are referred to a full-scale input FSR and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[6] This is the output from the internal band gap.
[7] The output voltage is internal and present on a dedicated multiplexer input.
[8] Unipolar mode: serial 16-bit straight binary.
Bipolar mode: serial 16-bit twos complement.
[9] Conversion results available immediately after completed conversion.
[10] With all digital inputs forced to VIO or GND as required.
[11] During acquisition phase.
[12] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

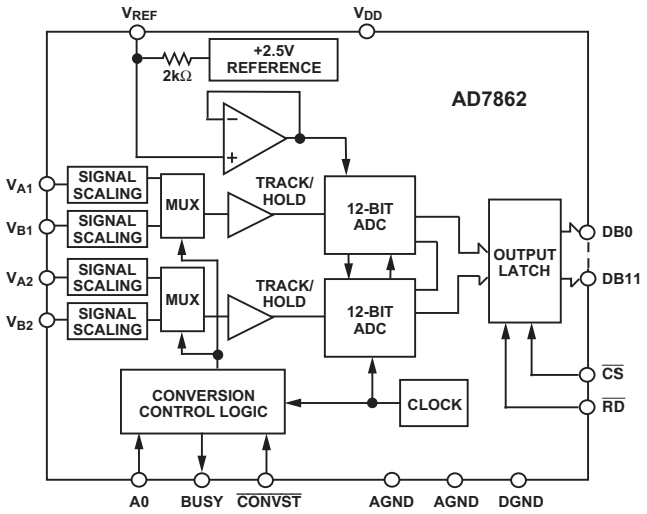
Simultaneous Sampling Dual 250 kSPS 12-Bit ADC

AD7862

FEATURES
Two Fast 12-Bit ADCs
Four Input Channels
Simultaneous Sampling & Conversion
4 μs Throughput Time
Single Supply Operation
Selection of Input Ranges:
±10 V for AD7862-10
±2.5 V for AD7862-3
0 V to 2.5 V for AD7862-2
High Speed Parallel Interface
Low Power, 60 mW typ
Power Saving Mode, 50 μW typ
Overvoltage Protection on Analog Inputs
14-Bit Pin Compatible Upgrade (AD7863)

APPLICATIONS
AC Motor Control
Uninterrupted Power Supplies
Data Acquisition Systems
Communications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7862 is a high speed, low power, dual 12-bit A/D converter that operates from a single +5 V supply. The part contains two 4 μs successive approximation ADCs, two track/hold amplifiers, an internal +2.5 V reference and a high speed parallel interface. There are four analog inputs that are grouped into two channels (A & B) selected by the A0 input. Each channel has two inputs (V_{A1} & V_{A2} or V_{B1} & V_{B2}) that can be sampled and converted simultaneously thus preserving the relative phase information of the signals on both analog inputs. The part accepts an analog input range of ±10 V (AD7862-10), ±2.5 V (AD7862-3) and 0–2.5 V (AD7862-2). Overvoltage protection on the analog inputs for the part allows the input voltage to go to ±17 V, ±7 V or +7 V, respectively, without causing damage.

A single conversion start signal ($\overline{CONVST}$) places both track/holds into hold simultaneously and initiates conversion on both inputs. The BUSY signal indicates the end of conversion, and at this time the conversion results for both channels are available to be read. The first read after a conversion accesses the result from V_{A1} or V_{B1}, while the second read accesses the result from V_{A2} or V_{B2}, depending on whether the multiplexer select A0 is low or high, respectively. Data is read from the part via a 12-bit parallel data bus with standard $\overline{CS}$ and $\overline{RD}$ signals.

In addition to the traditional dc accuracy specifications such as linearity, full-scale and offset errors, the part is also specified for dynamic performance parameters including harmonic distortion and signal-to-noise ratio.

The AD7862 is fabricated in Analog Devices' Linear Compatible CMOS (LC^2MOS) process, a mixed technology process that combines precision bipolar circuits with low power CMOS logic. It is available in 28-lead SSOP, SOIC and DIP.

PRODUCT HIGHLIGHTS

1. The AD7862 features two complete ADC functions allowing simultaneous sampling and conversion of two channels. Each ADC has a 2-channel input mux. The conversion result for both channels is available 3.6 μs after initiating conversion.
2. The AD7862 operates from a single +5 V supply and consumes 60 mW typ. The automatic power-down mode, where the part goes into power down once conversion is complete and "wakes up" before the next conversion cycle, makes the AD7862 ideal for battery-powered or portable applications.
3. The part offers a high speed parallel interface for easy connection to microprocessors, microcontrollers and digital signal processors.
4. The part is offered in three versions with different analog input ranges. The AD7862-10 offers the standard industrial input range of ±10 V; the AD7862-3 offers the common signal processing input range of ±2.5 V; while the AD7862-2 can be used in unipolar 0 V – +2.5 V applications.
5. The part features very tight aperture delay matching between the two input sample-and-hold amplifiers.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

AD7862–SPECIFICATIONS (V_{DD} = +5 V ± 5%, AGND = DGND = 0 V, REF = Internal. All Specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	A Version[1]	B Version	S Version	Units	Test Conditions/Comments
SAMPLE AND HOLD					
–3 dB Small Signal Bandwidth	3	3	3	MHz typ	
Aperture Delay	20	20	20	ns typ	
Aperture Jitter	100	100	100	ps typ	
Aperture Delay Matching	200	200	200	ps typ	
DYNAMIC PERFORMANCE[2]					f_{IN} = 100.0 kHz, f_S = 250 kSPS
Signal to (Noise+Distortion) Ratio[3]					
@ +25°C	70	71	70	dB min	
T_{MIN} to T_{MAX}	70	70	70	dB min	
Total Harmonic Distortion[3]	–78	–78	–78	dB max	
Peak Harmonic or Spurious Noise[3]	–85	–85	–85	dB typ	
Intermodulation Distortion[3]					fa = 49 kHz, fb = 50 kHz
2nd Order Terms	–85	–85	–85	dB typ	
3rd Order Terms	–85	–85	–85	dB typ	
Channel to Channel Isolation[3]	–80	–80	–80	dB max	f_{IN} = 100 kHz Sine Wave
DC ACCURACY					Any Channel
Resolution	12	12	12	Bits	
Minimum Resolution for which					
No Missing Codes are Guaranteed	12	12	12	Bits	
Relative Accuracy[3]	±1	±1	±1	LSB max	Typically 0.4 LSB
Differential Nonlinearity[3]	±1	±1	±1	LSB max	
Positive Gain Error[3]	±4	±3	±4	LSB max	
Positive Gain Error Match[3]	4	3	4	LSB max	
AD7862-10					
Negative Gain Error[3]	±4	±3	±4	LSB max	
Bipolar Zero Error	±4	±3	±4	LSB max	
Bipolar Zero Error Match	4	3	4	LSB max	
AD7862-3					
Negative Gain Error[3]	±4	±3	±4	LSB max	
Bipolar Zero Error	±4	±3	±4	LSB max	
Bipolar Zero Error Match	4	3	4	LSB max	
AD7862-2					
Unipolar Offset Error	+4	+3	+4	LSB max	
Unipolar Offset Error Match	4	3.5	4	LSB max	
ANALOG INPUTS					
AD7862-10					
Input Voltage Range	±10	±10	±10	Volts	Input
Input Resistance	24	24	24	kΩ min	
AD7862-3					
Input Voltage Range	±2.5	±2.5	±2.5	Volts	Input
Input Resistance	6	6	6	kΩ min	
AD7862-2					
Input Voltage Range	+2.5	+2.5	+2.5	Volts	Input
Input Current	500	500	500	nA max	
REFERENCE INPUT/OUTPUT					
REF IN Input Voltage Range	2.375/2.625	2.375/2.625	2.375/2.625	V min/V max	2.5 V ± 5%
REF IN Input Capacitance[4]	10	10	10	pF max	
REF OUT Output Voltage	2.5	2.5	2.5	V nom	
REF OUT Error @ +25°C	±10	±10	±10	mV max	
REF OUT Error T_{MIN} to T_{MAX}	±25	±25	±25	mV max	
REF OUT Temperature Coefficient	25	25	25	ppm/°C typ	
REF OUT Output Impedance	2	2	2	kΩ nom	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	V_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V ± 5%
Input Current, I_{IN}	±10	±10	±10	μA max	
Input Capacitance, C_{IN}[4]	10	10	10	pF max	

Parameter	A Version[1]	B Version	S Version	Units	Test Conditions/Comments
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	4.0	4.0	4.0	V min	I_{SOURCE} = 200 μA
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
DB11–DB0					
Floating-State Leakage Current	±10	±10	±10	μA max	
Floating-State Capacitance[4]	10	10	10	pF max	
Output Coding					
AD7862-10, AD7862-3					Twos Complement
AD7863-2					Straight (Natural) Binary
CONVERSION RATE					
Conversion Time	3.6	3.6	3.6	μs max	For Both Channels
Track/Hold Acquisition Time[2, 3]	0.3	0.3	0.3	μs max	
POWER REQUIREMENTS					
V_{DD}	+5	+5	+5	V nom	±5% for Specified Performance
I_{DD}					
Normal Mode	15	15	15	mA max	
Standby Mode	25	25	25	μA max	Logic Inputs = 0 V or V_{DD}
Power Dissipation					
Normal Mode	75	75	75	mW max	Typically 60 mW
Standby Mode	125	125	125	μW max	Typically 75 μW

NOTES
[1]Temperature ranges are as follows: A, B Versions: –40°C to +85°C; S Version: –55°C to +125°C.
[2] Performance measured through full channel (multiplexer, SHA and ADC).
[3]See Terminology.
[4]Sample tested @ +25°C to ensure compliance.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . –0.3 V to +7 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
AGND to DGND . . . . . ±0.3 V
Analog Input Voltage to AGND
AD7862-10 . . . . . ±17 V
AD7862-3 . . . . . ±7 V
AD7862-2 . . . . . +7 V
Reference Input Voltage to AGND . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Commercial (A, B Version) . . . . . –40°C to +85°C
Extended (S Version) . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
Plastic DIP Package, Power Dissipation . . . . . 670 mW
θ_{JA} Thermal Impedance . . . . . 116°C/W
Lead Temperature, (Soldering 10 sec) . . . . . +260°C
Ceramic DIP Package, Power Dissipation . . . . . 670 mW
θ_{JA} Thermal Impedance . . . . . 116°C/W
Lead Temperature, (Soldering 10 sec) . . . . . +260°C
SOIC Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 110°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C
SSOP Package, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 110°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Input Input	Relative Accuracy	Temperature Range	Package Description	Package Option
AD7862AR-10	±10 V	±1 LSB	–40°C to +85°C	28-Bit Small Outline Package	R-28
AD7862BR-10	±10 V	±1 LSB	–40°C to +85°C	28-Bit Small Outline Package	R-28
AD7862ARS-10	±10 V	±1 LSB	–40°C to +85°C	28-Bit Shrink Small Outline Package	RS-28
AD7862AN-10	±10 V	±1 LSB	–40°C to +85°C	28-Bit Plastic DIP	N-28
AD7862SQ-10	±10 V	±1 LSB	–55°C to +125°C	28-Bit Cerdip	Q-28
AD7862AR-3	±2.5 V	±1 LSB	–40°C to +85°C	28-Bit Small Outline Package	R-28
AD7862BR-3	±2.5 V	±1 LSB	–40°C to +85°C	28-Bit Small Outline Package	R-28
AD7862ARS-3	±2.5 V	±1 LSB	–40°C to +85°C	28-Bit Shrink Small Outline Package	RS-28
AD7862AN-3	±2.5 V	±1 LSB	–40°C to +85°C	28-Plastic DIP	N-28
AD7862AR-2	0 V to 2.5 V	±1 LSB	–40°C to +85°C	28-Bit Small Outline Package	R-28
AD7862ARS-2	0 V to 2.5 V	±1 LSB	–40°C to +85°C	28-Bit Shrink Small Outline Package	RS-28

MICROCHIP

dsPIC30F6011A/6012A/6013A/6014A

High-Performance, 16-bit Digital Signal Controllers

Note: This data sheet summarizes features of this group of dsPIC30F devices and is not intended to be a complete reference source. For more information on the CPU, peripherals, register descriptions and general device functionality, refer to the "*dsPIC30F Family Reference Manual*" (DS70046). For more information on the device instruction set and programming, refer to the "*dsPIC30F/33F Programmer's Reference Manual"* (DS70157).

High-Performance Modified RISC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set architecture
- Flexible addressing modes
- 83 base instructions
- 24-bit wide instructions, 16-bit wide data path
- Up to 144 Kbytes on-chip Flash program space
- Up to 48K instruction words
- Up to 8 Kbytes of on-chip data RAM
- Up to 4 Kbytes of nonvolatile data EEPROM
- 16 x 16-bit working register array
- Up to 30 MIPS operation:
  - DC to 40 MHz external clock input
  - 4 MHz-10 MHz oscillator input with PLL active (4x, 8x, 16x)
- Up to 41 interrupt sources:
  - 8 user-selectable priority levels
  - 5 external interrupt sources
  - 4 processor traps

DSP Features:

- Dual data fetch
- Modulo and Bit-Reversed modes
- Two 40-bit wide accumulators with optional saturation logic
- 17-bit x 17-bit single-cycle hardware fractional/ integer multiplier
- All DSP instructions are single cycle:
  - Multiply-Accumulate (MAC) operation
- Single-cycle ±16 shift

Peripheral Features:

- High-current sink/source I/O pins: 25 mA/25 mA
- Five 16-bit timers/counters; optionally pair up 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions:
- Data Converter Interface (DCI) supports common audio Codec protocols, including I^2S and AC'97
- 3-wire SPI modules (supports 4 Frame modes)
- I^2C™ module supports Multi-Master/Slave mode and 7-bit/10-bit addressing
- Two addressable UART modules with FIFO buffers
- Two CAN bus modules compliant with CAN 2.0B standard

Analog Features:

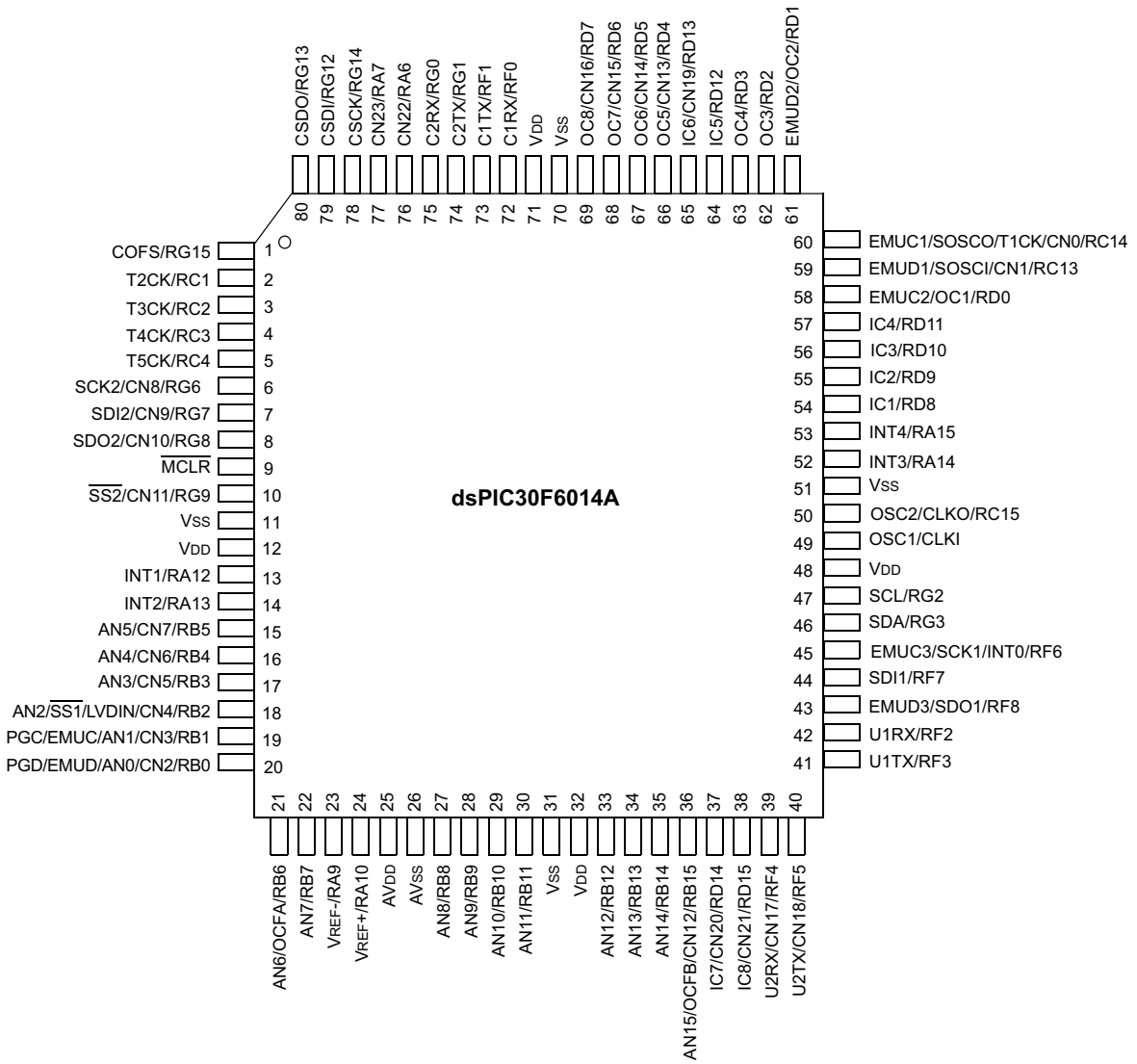
- 12-bit Analog-to-Digital Converter (ADC) with:
  - 200 Ksps conversion rate
  - Up to 16 input channels
  - Conversion available during Sleep and Idle
- Programmable Low-Voltage Detection (PLVD)
- Programmable Brown-out Reset

Special Microcontroller Features:

- Enhanced Flash program memory:
  - 10,000 erase/write cycle (min.) for industrial temperature range, 100K (typical)
- Data EEPROM memory:
  - 100,000 erase/write cycle (min.) for industrial temperature range, 1M (typical)
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Flexible Watchdog Timer (WDT) with on-chip low-power RC oscillator for reliable operation
- Fail-Safe Clock Monitor operation:
  - Detects clock failure and switches to on-chip low-power RC oscillator
- Programmable code protection
- In-Circuit Serial Programming™ (ICSP™)
- Selectable Power Management modes:
  - Sleep, Idle and Alternate Clock modes

Pin Diagrams (Continued)

80-Pin TQFP



Note: For descriptions of individual pins, see **Section 1.0 "Device Overview"**.

FIGURE 1-2: dsPIC30F6013A/6014A BLOCK DIAGRAM