POLITECNICO DI TORINO
ESAMI DI STATO PER L'ABILITAZIONE ALL'ESERCIZIO
DELLA PROFESSIONE DI INGEGNERE DELL'INFORMAZIONE IUNIOR

II Sessione 2016 - Sezione B
Settore dell'Informazione

PROVA PRATICA del 22 dicembre 2016

Il candidato svolga uno a scelta fra i seguenti temi proposti.
Gli elaborati prodotti dovranno essere stilati in forma chiara e ordinata.
La completezza, l'attinenza e la chiarezza espositiva costituiranno elementi di valutazione.

Tema n. 1

Il candidato progetti un sistema di monitoraggio di un velivolo, che tenga sotto controllo alcuni parametri, fra cui la temperatura del motore e le vibrazioni delle ali, avente preferibilmente le seguenti caratteristiche:

1) Temperature del motore:
    a. Intervallo di misura: +200°C ... +1000°C
    b. Accuratezza: +/- 1°C
    c. Unità di misura della memorizzazione: 1K
    d. Risoluzione della memorizzazione: 1/8 K
    e. Frequenza di acquisizione: 1 campione/s
2) vibrazioni:
    a. Intervallo di misura: -10 … +10 g
    b. Accuratezza: +/- 0.1 m/s^2
    c. Unità di misura della memorizzazione: 1 m/s^2
    d. Risoluzione della memorizzazione: 0.01 m/s^2
    e. Intervallo di frequenze utili: [1 Hz .. 100 Hz)
3) Capacità di memoria:
    a. Minimo 100 ore di volo
4) Sorgente di alimentazione:
    a. Il sistema dovrà funzionare con alimentazione esterna 12 +/- 2V DC; max 100mA.
    b. In assenza di alimentazione esterna, il sistema dovrà continuare a funzionare per almeno 10 ore con batterie ricaricabili interne che si ricaricano automaticamente in presenza di tensione di alimentazione.

Il candidato dovrà, nell'ordine:

1) Selezionare i trasduttori o sensori di temperatura e accelerazione e le batterie ricaricabili, eventualmente selezionandoli fra quelli proposti o, se si preferisce, qualunque altro modello commercialmente disponibile (in quest'ultimo caso, citando chiaramente modello e costruttore).
2) Sviluppare il progetto architetturale del sistema e predisporre uno schema a blocchi completo del sistema.
3) Si scelga un microcontrollore adatto al sistema, eventualmente scegliendo il modello MSP430F5438 della Texas Instruments di cui viene dato stralcio del datasheet.

4) Sviluppare lo schema elettrico di:
    a. Sensore di temperatura
    b. Sensore di vibrazione
    c. Alimentatore

    Tali da poter essere connessi direttamente all'alimentazione interna e agli ingressi analogici e/o digitali del microcontrollore.
5) Si imposti il diagramma di flusso del SW.
6) Si sviluppi, in qualsiasi linguaggio compilabile per microcontrollore la routine di inizializzazione dell'ADC del microcontrollore selezionato.

Allegati al testo d'esame:

1) Stralcio datasheet microcontrollore MSP430F5438
2) Stralcio user guide dell'ADC12 del MSP430F5438
3) Stralcio datasheet termocoppia TMPTJ
4) Stralcio datasheet sensore accelerazione LSM303D
5) Stralcio datasheet OP-AMP OPA378
6) Stralcio datasheet OP-AMP TSB611
7) Stralcio datasheet batteria ricaricabile

Segue: tabella temperatura-tensione termocoppia tipo K:

TERMOCOPPIA TIPO "K" (Cr-Al) SECONDO EN 60584-1 (ITS 90)

°C	0	-10	-20	-30	-40	-50	-60	-70	-80	-90	°C
	FEM termoelettrica in mV										
-200	-5,891	-6,035	-6,158	-6,262	-6,344	-6,404	-6,441	-6,458			-200
-100	-3,554	-3,852	-4,138	-4,411	-4,669	-4,913	-5,141	-5,354	-5,550	-5,730	-100
0	0,000	-0,392	-0,778	-1,156	-1,527	-1,889	-2,243	-2,587	-2,920	-3,243	0
°C	0	-10	-20	-30	-40	-50	-60	-70	-80	-90	°C

°C	0	10	20	30	40	50	60	70	80	90	°C
	FEM termoelettrica in mV										
0	0,000	0,397	0,798	1,203	1,612	2,023	2,436	2,851	3,267	3,682	0
100	4,096	4,509	4,920	5,328	5,735	6,138	6,540	6,941	7,340	7,739	100
200	8,138	8,539	8,940	9,343	9,747	10,153	10,561	10,971	11,382	11,795	200
300	12,209	12,624	13,040	13,457	13,874	14,293	14,713	15,133	15,554	15,975	300
400	16,397	16,820	17,243	17,667	18,091	18,516	18,941	19,366	19,792	20,218	400
500	20,644	21,071	21,497	21,924	22,350	22,776	23,203	23,629	24,055	24,480	500
600	24,905	25,330	25,755	26,179	26,602	27,025	27,447	27,869	28,289	28,710	600
700	29,129	29,548	29,965	30,382	30,798	31,213	31,628	32,041	32,453	32,865	700
800	33,275	33,685	34,093	34,501	34,908	35,313	35,718	36,121	36,524	36,925	800
900	37,326	37,725	38,124	38,522	38,918	39,314	39,708	10,101	40,490	40,885	900
1.000	41,276	41,665	42,053	42,440	42,826	43,211	43,595	43,978	44,359	44,740	1.000
1.100	45,119	45,497	45,873	46,249	46,623	46,995	47,367	47,737	48,105	48,473	1.100

		Type：SR674361P
		REV：1.0
		Date：2013-3-8

Specification Approval Sheet

Customer : Mikroe

Model : **SR674361P**

Type : **Li-polymer battery**

Specification: **3.7V/2000mAh**

signed by client	
Confirmed	
Checked	
Approved	

signed by manufacturer	
Prepared ：	**He lu**
Checked ：	
Approved ：	**Li Jin Yong**

Content

1. Battery type and scope

This Specification Approval Sheet is for rechargeable Li-polymer battery provided by Shirui Battery Co., LTD.

1.1 model：SR674361P

1.2 scope:

2. Basic characteristic and components of the battery

2.1 Basic performance parameter

S/N	Details	Parameters		Remarks
1	Rated voltage	3.7V		
2	Rated capacity	2000mAh		discharge with 0.2C to 2.75V after fully charge within 1h, measuring the discharge time
3	Limited charge voltage	4.2V		
4	Internal resistance	≤160mΩ		
5	charge mode	C.C/C.V.		
6	Charge time	6H		Standard charging 0.2C 400mA
7	Max Charge Current	2000mA		
8	Max discharge current	Continuous： 2000mA		
9	Working temperature	charging	0~45℃	
		discharging	-10~60℃	
10	Storage temperature	1 Month	-10~35℃	Charge to 40%~50% of capacity when storage
		6 months	-10~30℃	
11	Storage humidity	≤75％		relative humidity
12	Weight	Approx.45g		
13	ESD ability	Touch discharge ≥ 20000V		
		Air discharge≥20000V		
14	Cycle life	300 times		capacity≥80%

Note:If you need the battery protection parameters, please refer to PAGE 8.

2.2 Main components and parts

Materials	Model	Quantity	Related technical parameters	Manufacturer
Li-Polymer battery cell	SR674361P	1PCS	Please refer to the battery cell specification	/
Protection board	674361	1PCS		
Wire	JST-XHP-2 UL1007AWG24 Length 50mm	1PCS		

2.3 Reliable performance test

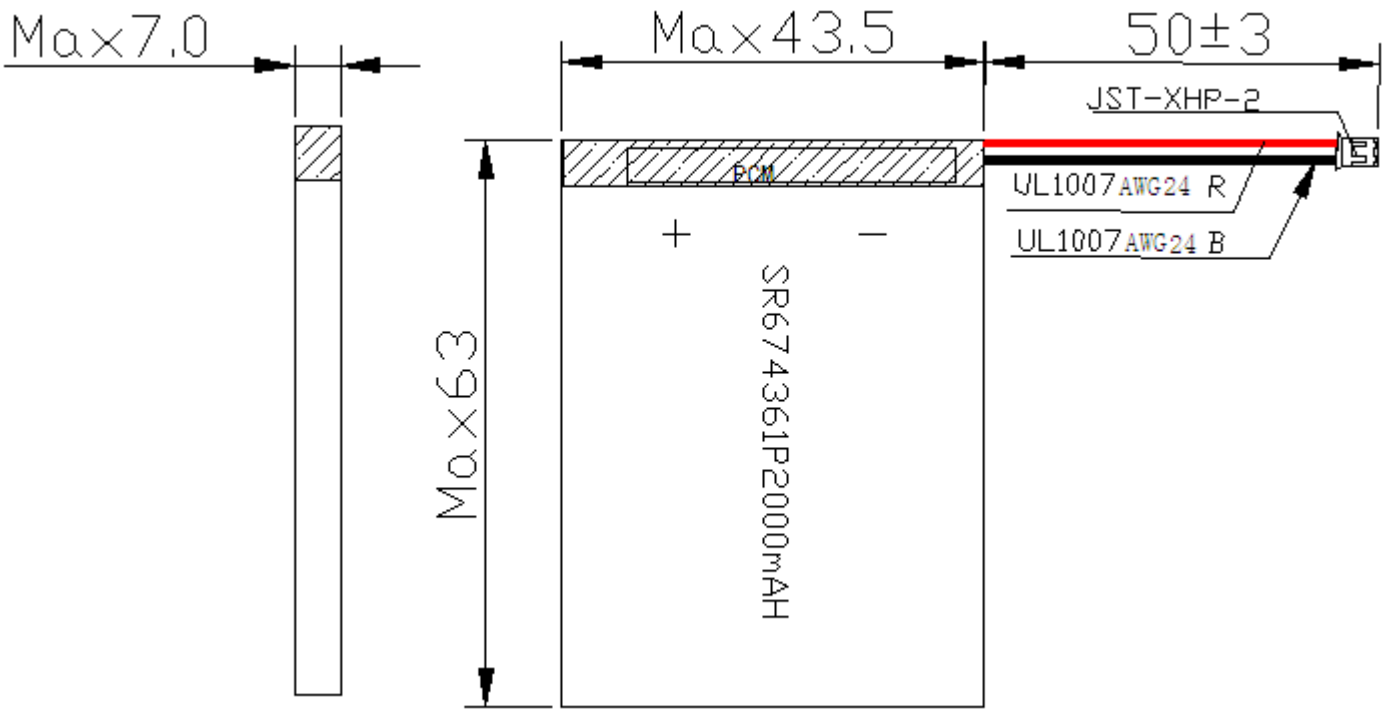
S/N	Inspection item	Standard	Testing Method
1	High temperature	No deformation, no rust, no fire or explosion; Discharge time ≥100mins with 0.5C_5A discharge	Place the battery in the environment of 55±2℃ for 2 hours after fully charge, then discharge with 0.5C_5A to cut-off voltage.
2	Low temperature	No deformation, no rust, no fire or explosion; Discharge time ≥ 3 hours with 0.2C_5A discharge at -20±2℃	After fully charge, place the battery in the environment of -20±2℃ for 16-24h, then discharge with 0.2C_5A to cut-off voltage. Then display the battery in 20±5℃ for 2 hours, observe the appearance of the battery.
		No deformation, no rust, no fire or explosion; Discharge time ≥ 3.5 hours with 0.2C_5A discharge at -10±2℃	After fully charge, place the battery in the environment of -10±2℃ for 16-24h, then discharge with 0.2C_5A to cut-off voltage. Then display the battery in 20±5℃ for 2 hours, observe the appearance of the battery.
3	Capability Retention	Discharge time ≥ 4.25h	After fully charged, store the battery at 20±5℃ for 28 days, then discharge with 0.2C_5A to cut-off voltage.

4	Constant humidity and heat	No deformation, no rust, no smoke or explosion. Discharge time ≥ 36 mins	After fully charge, place the battery in the environment of 40±2℃ and 90% - 95% Relative humidity for 48 hours, then place it in 20±5℃ for 2 hours, later, discharge with 1C_5A to cut-off voltage.
5	Vibration	No deformation, no rust, no smoke or explosion. Battery voltage ≥ 3.6V	Batteries are vibrated 30 minutes in three mutually perpendicular directions of X, Y, Z with amplitude of 0.38mm (10~55Hz) and the scanning rage of 1oct per minute.
6	Shock	No deformation, no smoke or explosion. Battery voltage ≥ 3.6V	Vibration test ended, place the battery in the directions of X.Y.Z three mutually perpendicular axis, and set pulse peak acceleration as 100m/s^2. Then shock the battery with frequency of 40 ~ 80 per minute. The duration of pulse is 16ms, Shock times: 2000 ± 10.
7	Free Drop	No leakage, no smoke or explosion, but a slight deformation. Discharge time ≥ 100mins at 0.5C_5A discharge	After shock test, the batteries are dropped on the 18-20mm hardwood on the concrete floor from 2000mm height as per positive and negative 6 direction of X, Y, Z. Each direction should drop one time. After test, batteries can be charged and discharged for at least three cycles.
8	Overcharge Protection	No explosion, no fire, no smoke or leakage	After fully charged, continue to charge the battery for 8 hours with C.C/C.V source. The constant voltage source sets to 2 times nominal voltage and constant current sets 2 C_5A.
9	Over-discharge Protection	No explosion, no fire, no smoke or leakage.	At 20±5℃, discharge the battery discharge with 0.2C_5A to cut-off voltage. Then, continuously discharge the battery with a 30Ω load resistance for 24 hours.
10	Short-circuit Protection	No explosion, no fire, no smoke or leakage; Batteries voltage is not less than N*3.6V after instantaneous charge.	After fully charge, short-circuit positive and negative electrode with 0.1Ω for 1 hour. Cut-off positive and negative electrode, then charge the battery at 0.5C_5A instantaneously for 5S.

11	Thermal Shock	No fire, No explosion	Battery is heated in a circulating air oven at a rate of (5±2)℃ per minute to 130℃, and then placed for 30 minutes at 130℃.
12	Overcharge	No fire, No explosion	Place battery connected thermocouple in a ventilated cabinet, connect the positive and negative to CC/CV source, and adjust constant current to $3C_5A$, and constant voltage to N*10V. Charge the battery to N*10V and current to 0 A. Then monitor the changes of temperature. If the temperature of battery drops to about 10℃ lower than the max temperature, test is finished.
13	Short circuit	No fire, No explosion. The out side temperature of the battery is less than 130℃.	Place battery connected thermocouple in a ventilated cabinet, short-circuit the positive and negative, then monitor the changes of temperature. If the temperature of battery drops to about 10℃ lower than the max temperature, test is finished.
14	Nail	No fire, No explosion	Put battery in the nail test platform. then, use a diameter 8 mm steel tip to poke through into hole. Finally, use a heavy hammer to blow the battery
15	Cycle life	Cycle life ≥ 300	At 20±5℃,charge battery with 0.5 C_5A to 4.2V and then charge it with constant voltage to the current less than 20mA. Stop charge and display for 0.5~1 hour. Then discharge it with 1 C_5A to cut-off voltage. Display for 0.5 ~1 hour, do next charge and discharge cycle. Repeat these steps. Stop it until the continuous two cycle discharge time is less than 48 minutes.

16	Storage	When it is stored for 3 month, fully charge it, then discharge it at 0.2 C_5A, discharge time is not less than 4 hours.	The storage test of battery should be selected a battery which is less than 3 month from production date to the date of experiment. Before storage, battery capacity should be full charged 40%~50% capacity, the ambient temperature is 20℃±5℃ and relative humidity is 45%-85%. After the storage expiration of battery, battery should be charged and discharged according to fully charged and discharged.

2.4 Dimension of the Battery



3. Specifications of Parts

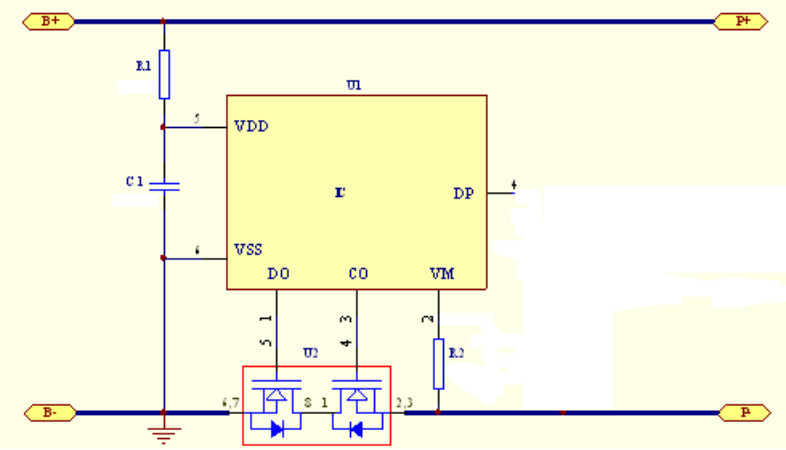
3.1: PCB: DW01/BMB101B02, 8205A

3.1. 1: General electric characteristic

Model of Protection IC:DW01/BMB101B02

Items	Specification	Remarks
Over-charging Protection Voltage	4.325V±0.1V	
Over-charging Return Voltage	4.1V±0.1V	
Over-discharge Protection Voltage	2.5V±0.1V	
Over-discharge Return Voltage	3.0V±0.1V	
Over-current Protection	2-5A	
Output short-circuit Protection Voltage	-1.2V~ -0.9V	
Detection Delay Time of Over-charging Protection	≤1.5S(Typical)	
Detection Delay Time of Over-discharging Protection	≤144mS(Typical)	
Detection Delay Time of Over-current Protection	≤9mS(Typical)	
Detection Delay Time of Output short-circuit Protection	≤320uS(Typical)	
Internal Resistance of Proper Functioning	≤2000mΩ	
Consume Current	≤6.0uA	
Operating Temperature	-20~70℃	

3.2 Electric schematic diagram of battery



3.3 : Components of the Fender Lists

No.	Name of the components	Position	Specification	Precision%	Dosage	Supplier	Remarks
1	PCB		674361	Negative tolerance	1		Latten
2	Internal Resistance	R1	100Ω ±5%/0402	±5	1		470Ω
3	Internal Resistance	R2	1KΩ ±5%/0402	±5	1		2KΩ
4	Capacity	C1	0.1μF/±10%/16V/0402	±20	1		0.1uF
5	Protect IC	U1	DW01/BMB101B02	/	1		SOT-23-6
6	MOS-FET	U2	8205A	/	1		

4 Specifications of the Cells

NO.	Items	Parameters		Tolerance	Term	Remark/ condition
1	Appearance	No mechanical damage, leakage , sink ,drum and so on		/	50cm distance under 40W daylight lamp	Visual
2	Dimensions	Length	61.0mm	Max 61.0mm	Digital caliper	
		Width	43.0mm	Max 43.0mm		
		Thickness	6.7mm	Max 6.7mm		
3	Voltage	≥3.80V		/	Multimeter	VC9801
4	Capacity	≥2000mAH		/	0.2C	
5	Internal resistance	≤80mΩ		/	1KHz	/
6	Consistency	Appearance quality is the same				
7	**Security**	**Correspond to related safety performance**				

Attentions

Danger

To prevent battery from weeping, fever, exploding ,please obey the rules as follows:
Do not immerse the battery into the water or the sea, Guard against Damp;
Do not approach the heat source, like fire or heater;
Please use the appointed charger when charging;
Do not transposition the +.- poles of the battery to charge;
Do not direct-connected the battery to alternating current power supply, or autoignition of the vehicle;
Do not discard the battery to the fire or hyperpyretic objects;
Do not use the conductor to lead the short circuit of the + -poles of the battery. Do not put the battery with metallic conductors to transport or store, like necklace, hairpin and so on;
Do not beat or throw the battery;
Do not impale the battery with needle or some other sharp things, do not strike it with weight;
As installed safety device in the battery, please do not resolve or change any other sections of the battery to protect the inherent safety functions;

Warnings

Do not put the battery to the microwave oven or pressure tank;
Do not use the battery with some chemical batteries (like dry battery) or different capacities and brands battery together, if the battery emits the smell, heat , changes color, be out of shape or appears any other abnormal phenomena during the charging or stored procedures, please get out the battery from the device or charger and stop using;
If can not recharge within the charging period, please not continue charging;
Put the battery to where the kids can not touch, if the kids swallow the battery , please seeing the doctor soon;
If the electrolyte of the battery into the eyes, do not rub ,should wash the eyes first ,then see the doctor;

Announcements

Do not put the battery under the high temperature places (like sunshine irradiation or car in the hot weather), or it will catch fire for the heat , reduce the performance and loss the life;

To insure the safety, the battery should install the safety device, please not use when the static electricity is more than we need when produce, or the safety device will lose efficacy and lead the overheating ,fracture, exploding and catching fire;

Please use the battery in normal as follows, or it will be overheating, caught fire , reduced performance and shorten the life;

Environment condition
(Temperature) Charging: 0~+45^{0}C
Discharging: -10~+60^{0}C
Store within 30 days: -10~+35^{0}C
Store within 90 days : -10~+30^{0}C

If the kids use the battery, they should use as the operation instruction manual and guarantee that it must be use in normal at any time;

.

If the battery weeps, the electrolytes stick on the skin or cloth, use the water to wash or running water to wash

To insure not install the battery wrong or wastage of the battery, please read the instruction carefully to install and dismounting;

If the battery will not be used for a long time ,please take out of the battery from the device and store in dry and shady places;

If there is sludge on the surface of the battery, please wipe up clean before using, or it will lead bad contact with the device.

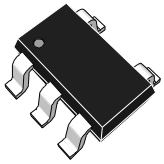
! Special Notice

Keep the cells in 50% charged state during long period storage. We recommend to charge the battery up to 50% of the total capacity every 3 months after receipt of the battery and maintain the voltage 3.7V~4.1V. And store the battery in cool and dry place.

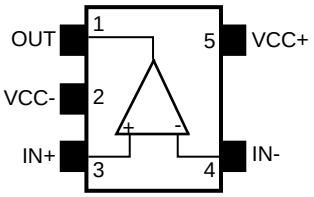
TSB611

Low-power, rail-to-rail output, 36 V operational amplifier

Datasheet - production data



SOT23-5



Features

- Low offset voltage: 1 mV max
- Low power consumption: 125 µA max. at 36 V
- Wide supply voltage: 2.7 to 36 V
- Gain bandwidth product: 560 kHz typ
- Unity gain stable
- Rail-to-rail output
- Input common mode voltage includes ground
- High tolerance to ESD: 4 kV HBM
- Extended temperature range: -40 °C to 125 °C
- Automotive qualification

Applications

- Industrial
- Power supplies
- Automotive

Description

The TSB611 single operational amplifier (op amp) offers an extended supply voltage operating range and rail-to-rail output. It also offers an excellent speed/power consumption ratio with 560 kHz gain bandwidth product while consuming less than 125 µA at 36V supply voltage.

The TSB611 operates over a wide temperature range from -40 °C to 125°C making this device ideal for industrial and automotive applications.

Thanks to its small package size, the TSB611 can be used in applications where space on the board is limited. It can thus reduce the overall cost of the PCB.

This is information on a product in full production.

www.st.com

1 Absolute maximum ratings and operating conditions

Table 1: Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage (1)	40	V
V_{id}	Differential input voltage (2)	$\pm V_{cc}$	
V_{in}	Input voltage	(V_{cc-}) - 0.2 to (V_{cc+}) + 0.2	
I_{in}	Input current (3)	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
R_{thja}	Thermal resistance junction to ambient (4)(5)	250	°C/W
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model (6)	4000	V
	MM: machine model (7)	200	
	CDM: charged device model (8)	1500	
	Latch-up immunity	200	mA

Notes:

(1)All voltage values, except differential voltage are with respect to network ground terminal.

(2)Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.

(3)Input current must be limited by a resistor in series with the inputs.

(4)R_{th} are typical values.

(5)Short-circuits can cause excessive heating and destructive dissipation.

(6)According to JEDEC standard JESD22-A114F.

(7)According to JEDEC standard JESD22-A115A.

(8)According to ANSI/ESD STM5.3.1.

Table 2: Operating conditions

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	2.7 to 36	V
V_{icm}	Common mode input voltage range	(V_{cc-}) - 0.1 to (V_{cc+}) - 1	
T_{oper}	Operating free air temperature range	-40 to 125	°C

2 Electrical characteristics

Table 3: Electrical characteristics at Vcc+ = 2.7 V with Vcc- = 0 V, Vicm = Vcc/2, Tamb = 25 °C, and RL = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-1		1	mV
		-40 °C < T< 125 °C	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C		1.8	6	µV/°C
I_{io}	Input offset current			1	5	nA
		-40 °C < T< 125 °C			10	
I_{ib}	Input bias current			5	10	
		-40 °C < T< 125 °C			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 V to V_{cc+} -1 V, V_{out} = V_{cc}/2	90	115		dB
		-40 °C < T< 125 °C	85			
A_{vd}	Large signal voltage gain	V_{out} = 0.5 V to (V_{cc+} - 0.5 V)	98	102		
		-40 °C < T< 125 °C	94			
V_{OH}	High level output voltage (voltage drop from V_{cc+})			13	25	mV
		-40 °C < T< 125 °C			30	
V_{OL}	Low level output voltage			26	30	
		-40 °C < T< 125 °C			35	
I_{out}	I_{sink}	V_{out} = V_{cc}	13	20		mA
		-40 °C < T< 125 °C	10			
	I_{source}	V_{out} = 0 V	20	28		
		-40 °C < T< 125 °C	7			
I_{CC}	Supply current (per channel)	No load, V_{out} = V_{cc}/2		92	110	µA
		-40 °C < T< 125 °C			125	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		480		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		430		
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		18		dB
SR+	Positive slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.13	0.18		V/µs
SR-	Negative slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.10	0.14		
e_n	Equivalent input noise voltage	f = 1 kHz		37		nV/√Hz
		f = 10 kHz		32		
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} - 1 V)/2, BW = 22 kHz, V_{out} = 1 V_{pp}		0.005		%

Table 4: Electrical characteristics at Vcc+ = 12 V with Vcc- = 0 V, Vicm = Vcc/2, Tamb = 25 °C, and RL = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage		-1		1	mV
		-40 °C < T< 125 °C	-1.6		1.6	
$\Delta V_{io}/\Delta T$	Input offset voltage drift	-40 °C < T< 125 °C		1.6	6	µV/°C
I_{io}	Input offset current			1	5	nA
		-40 °C < T< 125 °C			15	
I_{ib}	Input bias current			5	10	
		-40 °C < T< 125 °C			15	
CMR	Common mode rejection ratio: 20 log ($\Delta V_{icm}/\Delta V_{io}$)	V_{icm} = 0 V to V_{cc+} - 1 V, $V_{out} = V_{cc}/2$	95	126		dB
		-40 °C < T< 12 5°C	90			
SVR	Supply voltage rejection ratio: 20 log ($\Delta V_{cc}/\Delta V_{io}$)	V_{cc} = 2.8 to 12 V	95	124		
		-40 °C < T< 125 °C	90			
A_{vd}	Large signal voltage gain	V_{out} = 0.5 V to (V_{cc+} - 0.5 V)	105	115		
		-40 °C < T< 125 °C	100			
V_{OH}	High level output voltage drop from V_{cc+}			37	60	mV
		-40 °C < T< 125 °C			65	
V_{OL}	Low level output voltage			56	65	
		-40 °C < T< 125 °C			75	
I_{out}	I_{sink}	$V_{out} = V_{cc}$	24	35		mA
		-40 °C < T< 125 °C	10			
	I_{source}	V_{out} = 0 V	28	40		
		-40 °C < T< 125 °C	10			
I_{CC}	Supply current (per channel)	No load, $V_{out} = V_{cc}/2$		97	115	µA
		-40 °C < T< 125 °C			130	
AC performance						
GBP	Gain bandwidth product	R_L = 10 kΩ, C_L = 100 pF		510		kHz
F_u	Unity gain frequency	R_L = 10 kΩ, C_L = 100 pF		460		
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		60		Degrees
G_m	Gain margin	R_L = 10 kΩ, C_L = 100 pF		18		dB
SR+	Positive slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.13	0.19		V/µs
SR-	Negative slew rate	R_L = 10 kΩ, C_L = 100 pF, V_{out} = 0.5 V to V_{CC} - 0.5 V	0.11	0.15		
e_n	Equivalent input noise voltage	f = 1 kHz		31		nV/√Hz
		f = 10 kHz		30		
THD+N	Total harmonic distortion + noise	f_{in} = 1 kHz, Gain = 1, R_L = 100 kΩ, V_{icm} = (V_{cc} - 1 V)/2, BW = 22 kHz, V_{out} = 2 V_{pp}		0.004		%

Figure 1: Supply current vs. supply voltage at Vicm = VCC/2

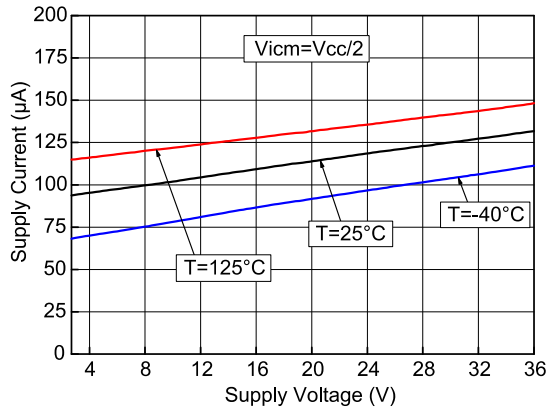


Figure 2: Input offset voltage distribution at VCC = 2.7 V

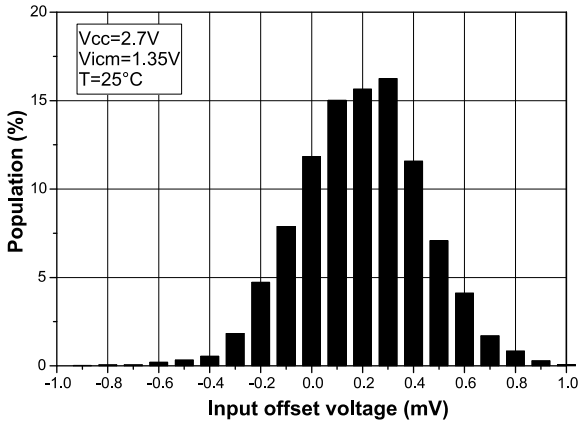


Figure 3: Input offset voltage distribution at VCC = 12 V

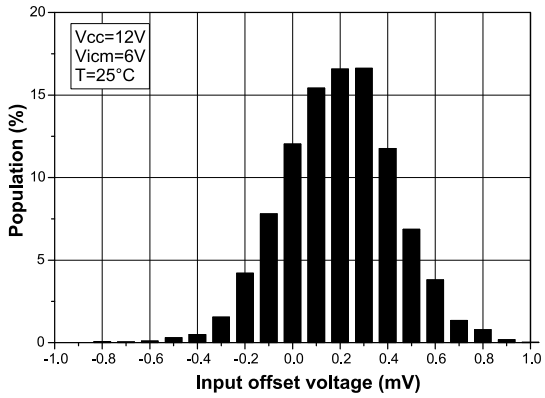


Figure 4: Input offset voltage distribution at VCC = 36 V

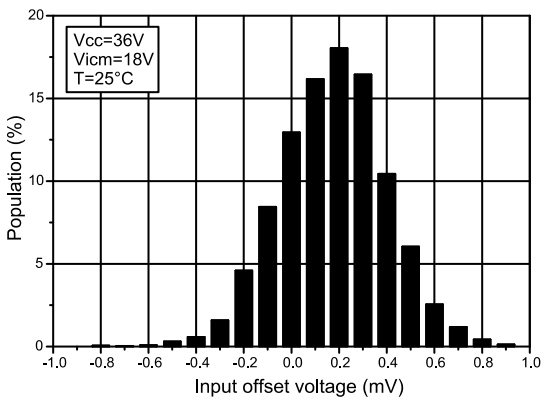


Figure 5: Input offset voltage vs. Temperature at VCC = 36 V

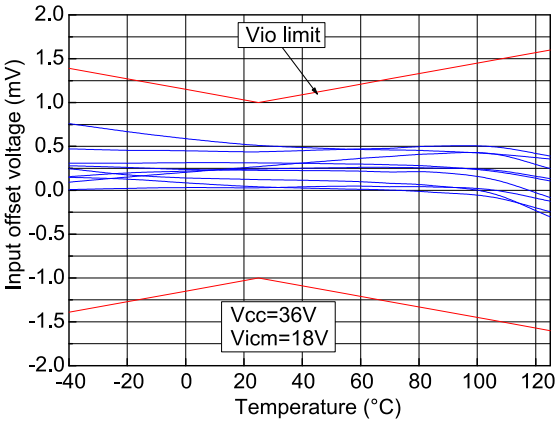


Figure 6: Input offset voltage temperature variation distribution at VCC = 36 V

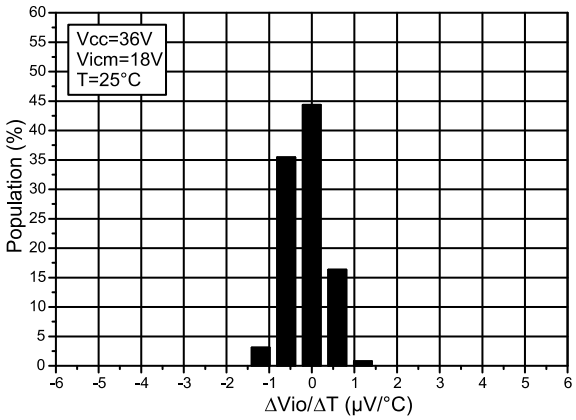


Figure 7: Input offset voltage vs. supply voltage

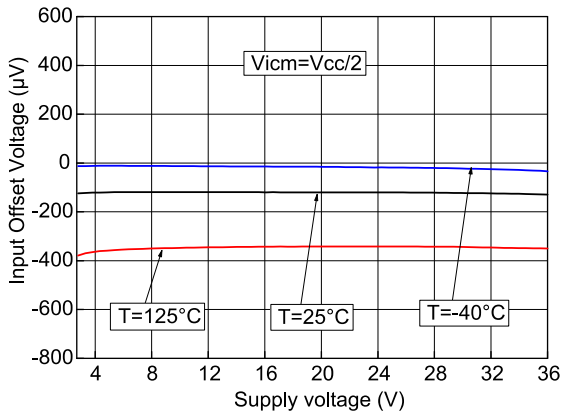


Figure 8: Input offset voltage vs. common-mode voltage at VCC = 2.7 V

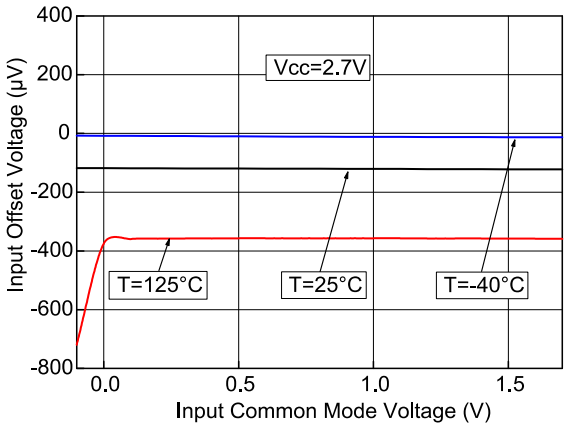


Figure 9: Input offset voltage vs. common-mode voltage at VCC = 36 V

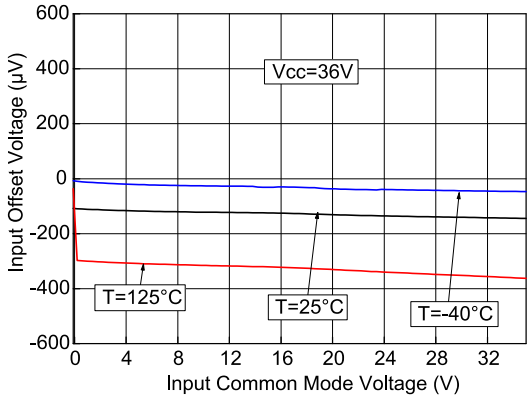


Figure 10: Input bias current vs. common mode voltage at VCC = 4 V

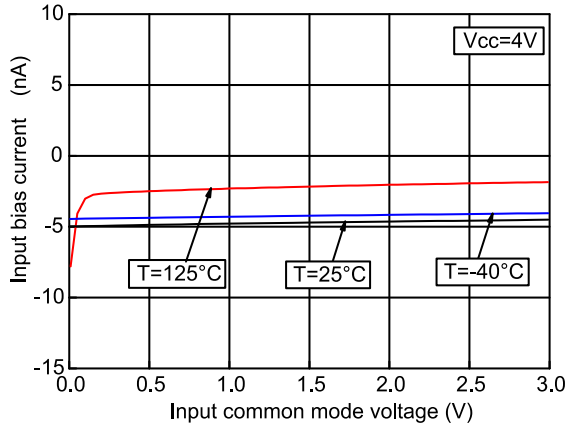


Figure 11: Input bias current vs. common mode voltage at VCC = 36 V

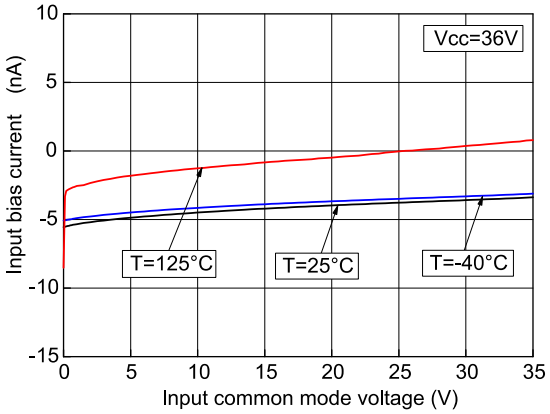
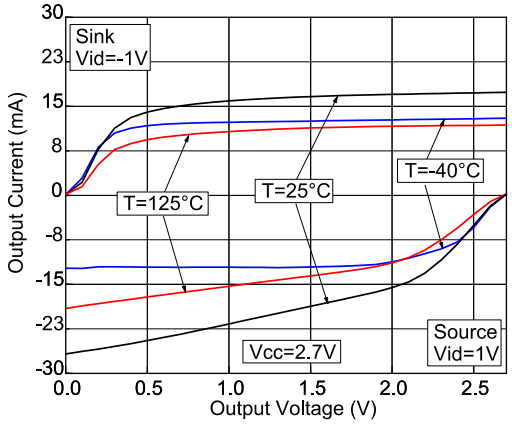


Figure 12: Output current vs. output voltage at VCC = 2.7 V



Low-Noise, 900kHz, RRIO, Precision OPERATIONAL AMPLIFIER Zerø-Drift Series

Check for Samples: OPA378 OPA2378

FEATURES

- **LOW NOISE**
  - **0.4μV_{PP}, 0.1Hz to 10Hz**
  - **20nV/√Hz at 1kHz**
- **ZERØ-DRIFT SERIES**
  - **LOW OFFSET VOLTAGE: 20μV**
  - **LOW OFFSET DRIFT: 0.1μV/°C**
- **QUIESCENT CURRENT: 125μA**
- **GAIN BANDWIDTH: 900kHz**
- **RAIL-TO-RAIL INPUT/OUTPUT**
- **EMI FILTERING**
- **SUPPLY VOLTAGE: 2.2V to 5.5V**
- ***micro*SIZE PACKAGES: SC70 and SOT23**

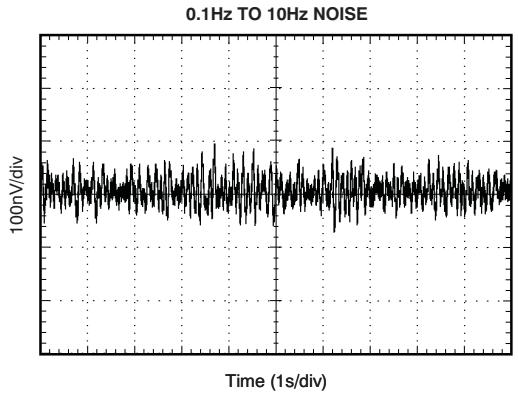
APPLICATIONS

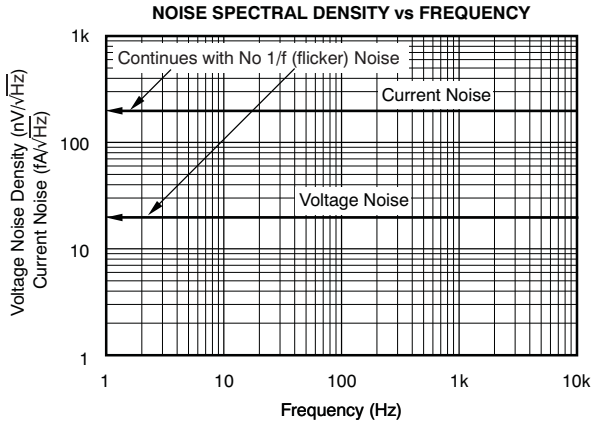
- **PORTABLE MEDICAL DEVICES**
  - **GLUCOSE METERS**
  - **OXYGEN METERING**
  - **HEART RATE MONITORS**
- **WEIGH SCALES**
- **BATTERY-POWERED INSTRUMENTS**
- **THERMOPILE MODULES**
- **HANDHELD TEST EQUIPMENT**
- **SENSOR SIGNAL CONDITIONING**

DESCRIPTION

The OPA378 and OPA2378 represent a new generation of Zerø-Drift, microPOWER™ operational amplifiers that use a proprietary auto-calibration technique to provide minimal input offset voltage (20μV) and offset voltage drift (0.1μV/°C). The combination of low input voltage noise, high gain bandwidth (900kHz), and low power (150μA max) enable these devices to achieve optimum performance for low-power precision applications. In addition, the excellent PSRR performance, coupled with a wide input supply range of 2.2V to 5.5V and rail-to-rail input and output, makes it an outstanding choice for single-supply applications that run directly from batteries without regulation.

The OPA378 (single version) is available in both a *micro*SIZE SC70-5 and a SOT23-5 package. The OPA2378 (dual version) is offered in a SOT23-8 package. All versions are specified for operation from –40°C to +125°C.





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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA378	SOT23-5	DBV	OAZI
OPA378	SC70-5	DCK	BTS
OPA2378	SOT23-8	DCN	OCAI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

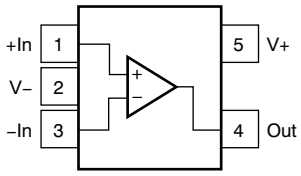
Over operating free-air temperature range (unless otherwise noted).

		OPA378, OPA2378	UNIT
Supply Voltage, V_S = (V+) – (V–)		+7	V
Signal Input Terminals	Voltage(2)	(V–) – 0.3 ≤ V_{IN} ≤ (V+) + 0.3	V
	Current(2)	±10	mA
Output Short-Circuit(3)		Continuous	
Operating Temperature, T_A		–55 to +150	°C
Storage Temperature, T_A		–65 to +150	°C
Junction Temperature, T_J		+150	°C
ESD Ratings	Human Body Model (HBM)	4000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

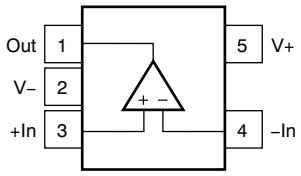
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

PIN CONFIGURATIONS

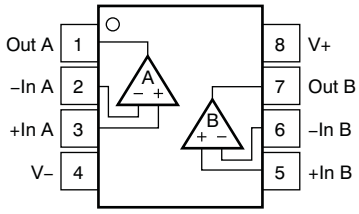
OPA378
SC70-5
(TOP VIEW)



OPA378
SOT23-5
(TOP VIEW)



OPA2378
SOT23-8
(TOP VIEW)



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ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA378, OPA2378 MIN	OPA378, OPA2378 TYP	OPA378, OPA2378 MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage, OPA378	V_{OS}	V_{CM} = V–		20	50	µV
vs Temperature	**dV_{OS}/dT**			**0.1**	**0.25**	**µV/°C**
Input Offset Voltage, OPA2378				20	70	µV
vs Temperature	**dV_{OS}/dT**	**-40°C to +125°C**		**0.25**	**0.4**	**µV/°C**
		–40°C to +85°C		0.15	0.25	µV/°C
vs Power Supply, OPA378	PSRR	V_{CM} = 0V, V_S = +2.2V to +5.5V		1.5	5	µV/V
over Temperature		**V_{CM} = 0V, V_S = +2.2V to +5.5V**		**3**	**8**	**µV/V**
vs Power Supply, OPA2378		V_{CM} = 0V, V_S = +2.2V to +5.5V			10	µV/V
over Temperature		**V_{CM} = 0V, V_S = +2.2V to +5.5V**		**3**	**13**	**µV/V**
Channel Separation (Dual Version)		At dc		135		dB
INPUT BIAS CURRENT						
Input Bias Current, OPA378	I_B			±150	±550	pA
Input Bias Current, OPA2378				±150	±670	pA
over Temperature, OPA378 and OPA2378					**±2**	**nA**
Input Offset Current, OPA378	I_{OS}			±0.3	±1.1	nA
Input Offset Current, OPA2378				±0.3	±1.34	nA
NOISE						
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz, V_S = +5.5V		0.4		μV_{PP}
Input Voltage Noise Density	e_n	f = 1kHz		20		$nV/\sqrt{Hz}$
Input Current Noise	i_n	f = 10Hz		200		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) – 0.05		(V+) + 0.05	V
Common-Mode Rejection Ratio	CMRR	(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 5.5V	100	112		dB
		(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 2.2V	94	106		dB
over Temperature		**(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 5.5V**	**96**			**dB**
		(V–) – 0.05V < V_{CM} < (V+) + 0.05V, V_S = 2.2V	**90**			**dB**
INPUT CAPACITANCE						
Differential	C_{IN}			4		pF
Common-Mode				5		pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	50mV < V_O < (V+) – 50mV, R_L = 100kΩ	110	134		dB
		100mV < V_O < (V+) – 100mV, R_L = 10kΩ	110	130		dB
over Temperature		**100mV < V_O < (V+) – 100mV, R_L = 10kΩ**	**106**			**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			900		kHz
Slew Rate	SR	G = +1		0.4		V/µs
Settling Time 0.1%	t_S	V_S = 5.5V, 2V Step, G = +1		7		µs
Settling Time 0.01%	t_S	V_S = 5.5V, 2V Step, G = +1		9		µs
Overload Recovery Time		V_{IN} × Gain > V_S		4		µs
THD + Noise	THD + N	V_S = 5V, V_O = $3V_{PP}$, G = +1, f = 1kHz		0.003		%

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ELECTRICAL CHARACTERISTICS: V_S = +2.2V to +5.5V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA378, OPA2378 MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail, OPA378	V_O	R_L = 10kΩ		6	8	mV
over Temperature		**R_L = 10kΩ**		**8**	**13**	**mV**
Voltage Output Swing from Rail, OPA2378	V_O	R_L = 10kΩ		6	10	mV
over Temperature		**R_L = 10kΩ**		**8**	**15**	**mV**
Voltage Output Swing from Rail		R_L = 100kΩ		0.7	2	mV
over Temperature		**R_L = 100kΩ**			**3**	**mV**
Short-Circuit Current	I_{SC}			±30		mA
Capacitive Load Drive	C_{LOAD}			See Figure 18		pF
Open-Loop Output Impedance	Z_O			See Figure 23		Ω
POWER SUPPLY						
Specified Voltage Range	V_S		2.2		5.5	V
Quiescent Current (per Amplifier)	I_Q	I_O = 0mA, V_S = +5.5V		125	150	µA
over Temperature					**165**	**µA**
TEMPERATURE RANGE						
Specified Range			–40		+125	°C
Operating Range			–55		+150	°C
Thermal Resistance	θ_{JA}					°C/W
SOT23-5				200		°C/W
SC70-5				250		°C/W
SOT23-8				100		°C/W

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TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

0.1Hz TO 10Hz NOISE

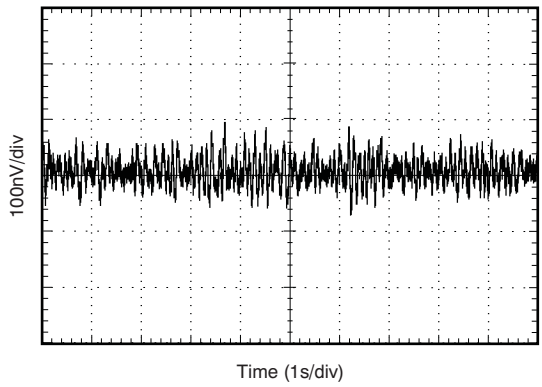

Figure 1.

INPUT CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

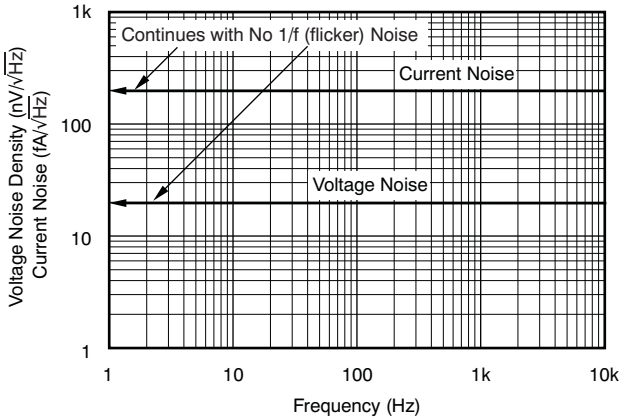

Figure 2.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

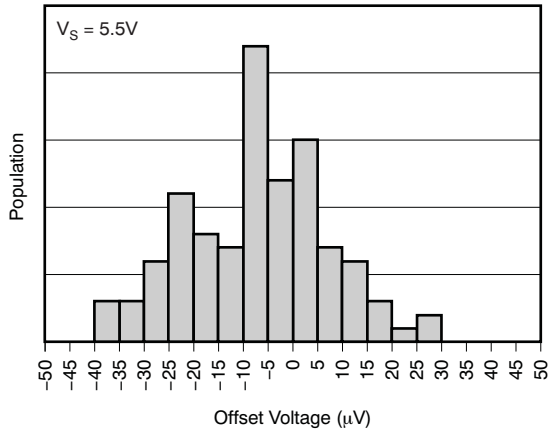

Figure 3.

OFFSET VOLTAGE DRIFT DISTRIBUTION

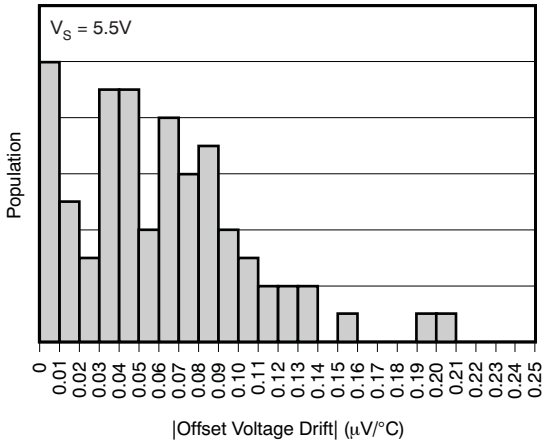

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 10kΩ, V_S = +5.5V and V_{OUT} = V_S/2, unless otherwise noted.

OFFSET VOLTAGE vs TEMPERATURE

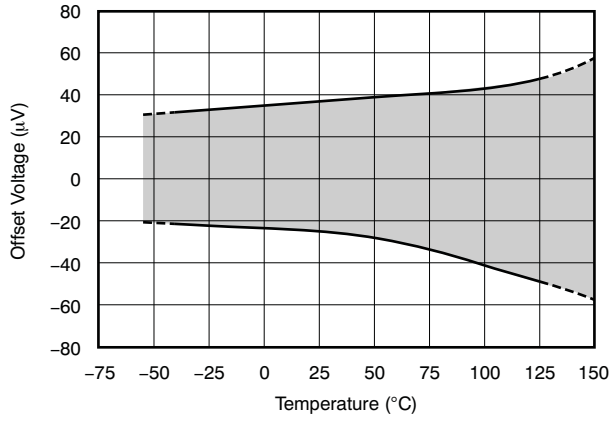

Figure 5.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

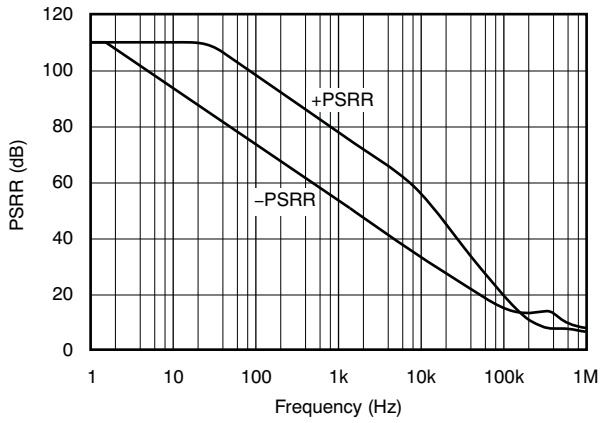

Figure 6.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

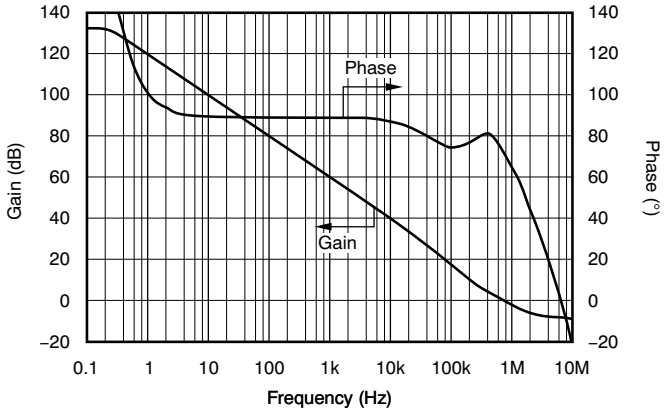

Figure 7.

OPEN-LOOP GAIN vs TEMPERATURE

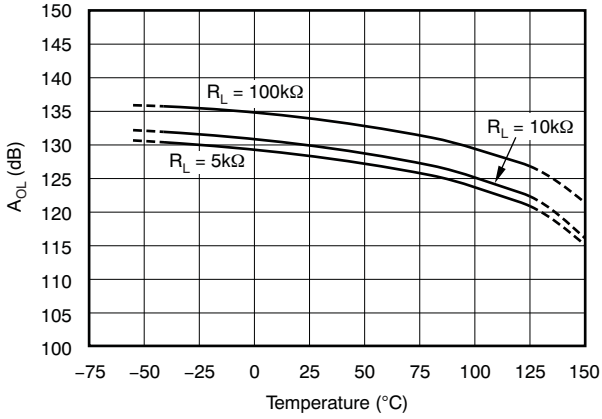

Figure 8.

COMMON-MODE REJECTION RATIO vs FREQUENCY

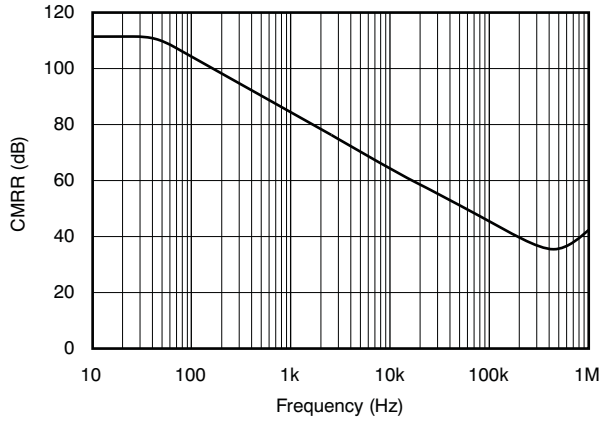

Figure 9.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs TEMPERATURE

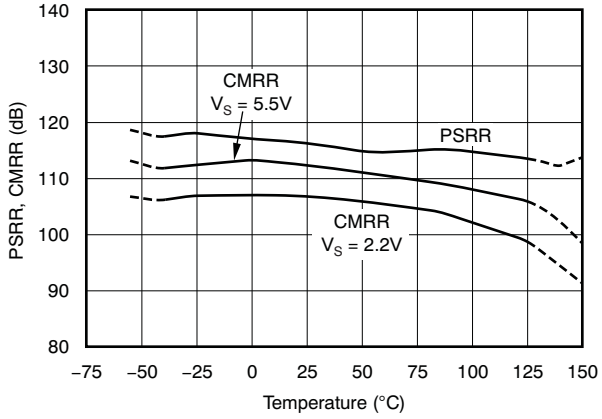

Figure 10.

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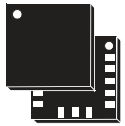
LSM303D

Ultra-compact high-performance eCompass module: 3D accelerometer and 3D magnetometer

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- 3 magnetic field channels and 3 acceleration channels
- ±2/±4/±8/±12 gauss magnetic full scale
- ±2/±4/±6/±8/±16 *g* linear acceleration full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 2.16 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators for free-fall, motion detection and magnetic field detection
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK®, RoHS and “Green” compliant

Applications

- Tilt-compensated compasses
- Map rotation
- Position detection
- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Pedometers
- Intelligent power saving for handheld devices
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LSM303D is a system-in-package featuring a 3D digital linear acceleration sensor and a 3D digital magnetic sensor.

The LSM303D has linear acceleration full scales of ±2*g* / ±4*g* / ±6*g* / ±8*g* / ±16*g* and a magnetic field full scale of ±2 / ±4 / ±8 / ±12 gauss.

The LSM303D includes an I^2C serial bus interface that supports standard and fast mode (100 kHz and 400 kHz) and SPI serial standard interface.

The system can be configured to generate an interrupt signal for free-fall, motion detection and magnetic field detection. Thresholds and timing of interrupt generators are programmable by the end user.

Magnetic and accelerometer blocks can be enabled or put into power-down mode separately.

The LSM303D is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

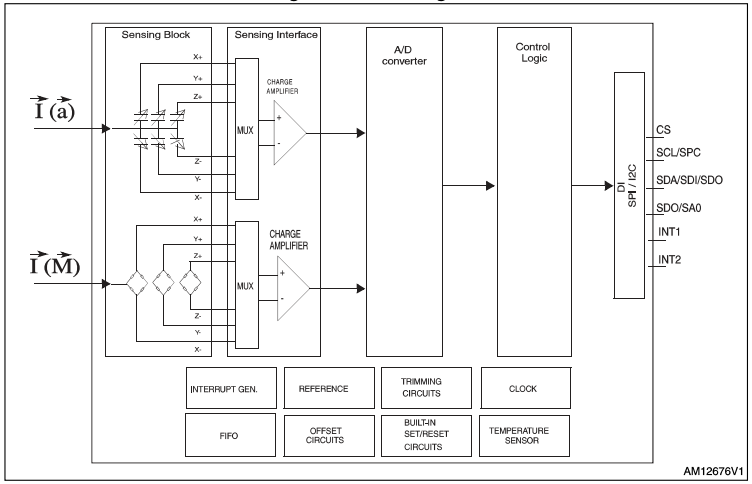
Part number	Temperature range [°C]	Package	Packaging
LSM303D	-40 to +85	LGA-16	Tray
LSM303DTR	-40 to +85	LGA-16	Tape and reel

This is information on a product in full production.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

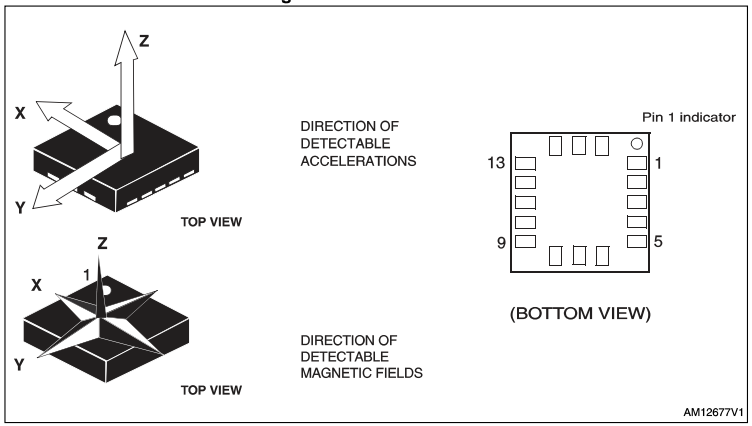


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	SETC	S/R capacitor connection (C_2)
3	SETP	S/R capacitor connection (C_2)
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0 V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	SPI serial data output (SDO) I^2C less significant bit of the device address (SA0)
8	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	INT 2	Interrupt 2
10	Reserved	Connect to GND
11	INT 1	Interrupt 1
12	GND	0 V supply
13	GND	0 V supply
14	Vdd	Power supply
15	C1	Capacitor connection (C_1)
16	GND	0 V supply

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]			±2		*g*
				±4		
				±6		
				±8		
				±16		
M_FS	Magnetic measurement range			±2		gauss
				±4		
				±8		
				±12		
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 *g*		0.061		mg/LSB
		Linear acceleration FS = ±4 *g*		0.122		
		Linear acceleration FS = ±6 *g*		0.183		
		Linear acceleration FS = ±8 *g*		0.244		
		Linear acceleration FS = ±16 *g*		0.732		
M_So	Magnetic sensitivity	Magnetic FS = ±2 gauss		0.080		mgauss/ LSB
		Magnetic FS = ±4 gauss		0.160		
		Magnetic FS = ±8 gauss		0.320		
		Magnetic FS = ±12 gauss		0.479		
LA_TCSo	Linear acceleration sensitivity change vs. temperature			±0.01		%/°C
M_TCSo	Magnetic sensitivity change vs. temperature			±0.05		%/°C
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy[3],[4]			±60		m*g*
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature	Max delta from 25 °C		±0.5		m*g*/°C
LA_An	Linear acceleration noise density	Linear acceleration FS = 2*g*; ODR = 100 Hz		150		$ug/(\sqrt{Hz})$
M_R	Magnetic noise density	Magnetic FS = 2 gauss; LR setting CTRL5 (M_RES [1,0]) = 00b		5		mgauss/ RMS

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
M_CAS	Magnetic cross-axis sensitivity	Cross field = 0.5 gauss Applied = ±3 gauss		±1		%FS/ gauss
M_EF	Maximum exposed field	No permanent effect on sensor performance			10000	gauss
M_DF	Magnetic disturbance field	Sensitivity starts to degrade. Automatic S/R pulse restores the sensitivity(5)			20	gauss
LA_ST	Linear acceleration self-test positive difference(6)	±2 *g* range, X-, Y-axis AST = 1 see *Table 37*	70		1700	mg
		±2 *g* range, Z-axis AST = 1 see *Table 37*	70		1700	
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. Set/reset pulse is automatically applied at each conversion cycle.
6. "Self-test output change" is defined as: $OUTPUT[mg]_{(CTRL2\ AST\ bit\ =1)}$ - $OUTPUT[mg]_{(CTRL2\ AST\ bit\ =0)}$.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[b].

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		8		LSB/°C
TODR	Temperature refresh rate			M_ODR [2:0](2)		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Refer to *Table 47: Magnetic data rate configuration*.

b. The product is factory calibrated at 2.5 V.

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.16		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	
Idd	eCompass(2) current consumption in normal mode(3)	LR setting CTRL5 (M_RES [1,0]) = 00b, see *Table 45*		300		µA
IddSL	Current consumption in power-down mode(4)			1		µA
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. eCompass: accelerometer and magnetic sensor.
3. Magnetic sensor setting ODR = 6.25 Hz, accelerometer sensor ODR = 50 Hz and magnetic high-resolution setting.
4. Linear accelerometer and magnetic sensor in power-down mode.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL/SPC, SDA/SDI/SDO, SDO/SA0, CS)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Set/reset pulse

The set/reset pulse is an automatic operation performed before each magnetic acquisition cycle to recover the initial magnetization state of the sensor and therefore the linearity of the sensor itself.

3.2 Sensitivity

3.2.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.2.2 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying a magnetic field of 1 *gauss* to it.

3.3 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two’s complement). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Zero-*g* level change vs. temperature”. The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3.4 Zero-*gauss* level

Zero-*g*auss level offset describes the deviation of an actual output signal from the ideal output if no magnetic field is present. Thanks to the set/reset pulse and to the magnetic sensor read-out chain, the offset is dynamically cancelled. The Zero-*g*auss level does not show any dependencies on temperature and power supply.

4 Functionality

4.1 Self-test

The self-test allows checking the linear acceleration sensor functionality without moving the sensor. The self-test function is off when the self-test bit (AST) is programmed to '0'. When the self-test bit is programmed to '1', an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Section 2.1*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.2 Temperature sensor

The LSM303D features an internal temperature sensor. Temperature data can be enabled by setting the TEMP_EN bit on the *CTRL5 (24h)* register to 1.

Both the TEMP_OUT_H and TEMP_OUT_L registers must be read.

Temperature data is stored inside *TEMP_OUT_L (05h), TEMP_OUT_H (06h)* as two's complement data in 12-bit format, right-justified.

The output data rate of the temperature sensor is set by M_ODR [2:0] in *CTRL5 (24h)* and is equal to the magnetic sensor output data rate.

4.3 FIFO

The LSM303D embeds an acceleration data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, as the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work according to four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits. Programmable threshold level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT 1 or INT 2 pin.

Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 5*, for each channel only the first address is used. The remaining FIFO slots are empty.

FIFO mode

In FIFO mode, data from X, Y and Z channels are stored in the FIFO. A FIFO threshold interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it is full. When full, the FIFO stops collecting data from the input channels.

Stream mode

In Stream mode, data from X, Y and Z measurements are stored in the FIFO. A FIFO threshold interrupt can be enabled and set as in FIFO mode.The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive.

Stream-to-FIFO mode

In Stream-to-FIFO mode, data from X, Y and Z measurements are stored in the FIFO. A FIFO threshold interrupt can be enabled in order to be raised when the FIFO is filled to the level specified by the internal register. The FIFO continues filling until it's full. When full, the FIFO discards the older data as the new arrive. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

Bypass-to-Stream mode

In Bypass-to-Stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to *IG_CFG1 (30h)* register events), the FIFO starts operating in Stream mode.

Retrieving data from FIFO

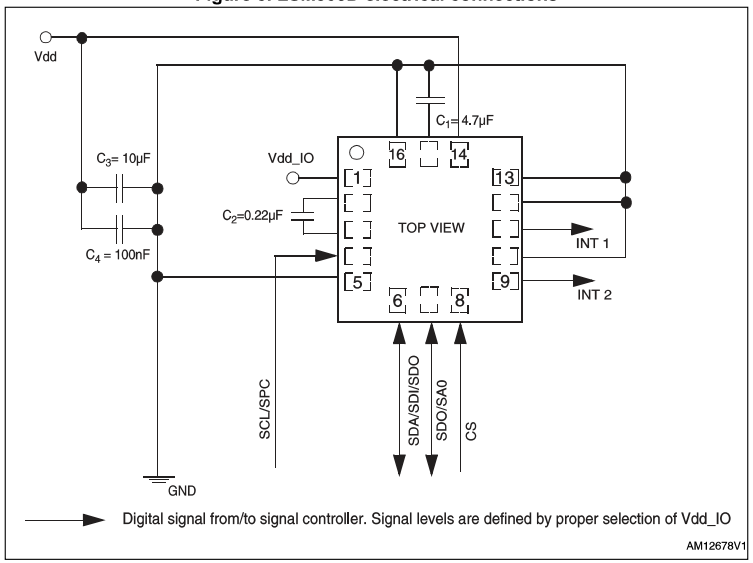
FIFO data is read from the OUT_X_A, OUT_Y_A and OUT_Z_A registers. When the FIFO is in Stream, Stream-to-FIFO, Bypass-to-Stream or FIFO mode, a read operation to the OUT_X_A, OUT_Y_A or OUT_Z_A registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the OUT_X_A, OUT_Y_A and OUT_Z_A registers and both single read and read_burst operations can be used.

4.4 Factory calibration

The IC interface is factory calibrated. The trim values are stored inside the device in nonvolatile memory. Anytime the device is turned on, the trimming parameters are downloaded into the registers to be used during normal operation. This allows the user to use the device without further calibration.

5 Application hints

Figure 5. LSM303D electrical connections



5.1 External capacitors

The C_1 and C_2 external capacitors should be low SR value ceramic type construction (typ. recommended value 200 mΩ). Reservoir capacitor C_1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C_2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C_4 = 100 nF ceramic, C_3 = 10 µF Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*).

The functionality of the device and the measured acceleration/magnetic field data is selectable and accessible through the I^2C/SPI interfaces.

The functions, the threshold and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I^2C/SPI interfaces.

5.2 Pull-up resistors

If an I^2C interface is used, pull-up resistors (recommended value 10 kΩ) must be placed on the two I^2C bus lines.

7 Output register mapping

The table below provides a listing of the 8-bit registers embedded in the device and the corresponding addresses.

Table 16. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved	--	00-04	--	--	Reserved
TEMP_OUT_L	r	05	000 0101	Output	
TEMP_OUT_H	r	06	000 0110	Output	
STATUS_M	r	07	000 0111	Output	
OUT_X_L_M	r	08	000 1000	Output	
OUT_X_H_M	r	09	000 1001	Output	
OUT_Y_L_M	r	0A	000 1010	Output	
OUT_Y_H_M	r	0B	000 1011	Output	
OUT_Z_L_M	r	0C	000 1100	Output	
OUT_Z_H_M	r	0D	000 1101	Output	
Reserved	--	0E	000 1110	--	Reserved
WHO_AM_I	r	0F	000 1111	01001001	
Reserved	--	10-11	--	--	Reserved
INT_CTRL_M	rw	12	001 0010	11101000	
INT_SRC_M	r	13	001 0011	Output	
INT_THS_L_M	rw	14	001 0100	00000000	
INT_THS_H_M	rw	15	001 0101	00000000	
OFFSET_X_L_M	rw	16	001 0110	00000000	
OFFSET_X_H_M	rw	17	001 0111	00000000	
OFFSET_Y_L_M	rw	18	001 01000	00000000	
OFFSET_Y_H_M	rw	19	001 01001	00000000	
OFFSET_Z_L_M	rw	1A	001 01010	00000000	
OFFSET_Z_H_M	rw	1B	001 01011	00000000	
REFERENCE_X	rw	1C	001 01100	00000000	
REFERENCE_Y	rw	1D	001 01101	00000000	
REFERENCE_Z	rw	1E	001 01110	00000000	
CTRL0	rw	1F	001 1111	00000000	
CTRL1	rw	20	010 0000	00000111	
CTRL2	rw	21	010 0001	00000000	

Table 16. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
CTRL3	rw	22	010 0010	00000000	
CTRL4	rw	23	010 0011	00000000	
CTRL5	rw	24	010 0100	00011000	
CTRL6	rw	25	010 0101	00100000	
CTRL7	rw	26	010 0110	00000001	
STATUS_A	r	27	010 0111	Output	
OUT_X_L_A	r	28	010 1000	Output	
OUT_X_H_A	r	29	010 1001	Output	
OUT_Y_L_A	r	2A	010 1010	Output	
OUT_Y_H_A	r	2B	010 1011	Output	
OUT_Z_L_A	r	2C	010 1100	Output	
OUT_Z_H_A	r	2D	010 1101	Output	
FIFO_CTRL	rw	2E	010 1110	00000000	
FIFO_SRC	r	2F	010 1111	Output	
IG_CFG1	rw	30	011 0000	00000000	
IG_SRC1	r	31	011 0001	Output	
IG_THS1	rw	32	011 0010	00000000	
IG_DUR1	rw	33	011 0011	00000000	
IG_CFG2	rw	34	011 0100	00000000	
IG_SRC2	r	35	011 0101	Output	
IG_THS2	rw	36	011 0110	00000000	
IG_DUR2	rw	37	011 0111	00000000	
CLICK_CFG	rw	38	011 1000	00000000	
CLICK_SRC	r	39	011 1001	Output	
CLICK_THS	rw	3A	011 1010	00000000	
TIME_LIMIT	rw	3B	011 1011	00000000	
TIME _LATENCY	rw	3C	011 1100	00000000	
TIME_WINDOW	rw	3D	011 1101	00000000	
ACT_THS	rw	3E	011 1110	00000000	
ACT_DUR	rw	3F	011 1111	00000000	

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration and magnetic data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

8.1 TEMP_OUT_L (05h), TEMP_OUT_H (06h)

Temperature sensor data. Temperature data is stored as two's complement data in 12-bit format, right-justified.

Refer to *Section 4.2* for details on how to enable and read the temperature sensor output data.

8.2 STATUS_M (07h)

Table 17. STATUS_M register

ZYXMOR/ Tempor	ZMOR	YMOR	XMOR	ZYXMDA / Tempda	ZMDA	YMDA	XMDA

Table 18. STATUS_M register description

ZYXMOR/ Tempor	Magnetic X, Y and Z-axis and temperature data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous data) Temperature data overrun if T_ONLY bit in *CTRL7 (26h)* is set to '1'. Default value: 0.
ZMOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YMOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XMOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXMDA/ Tempda	X, Y and Z-axis and temperature new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available) Temperature new data available if the T_ONLY bit in *CTRL7 (26h)* is set to '1'.
ZMDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YMDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XMDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.3 OUT_X_L_M (08h), OUT_X_H_M (09h)

X-axis magnetic data. The value is expressed in 16-bit as two's complement.

8.4 OUT_Y_L_M (0Ah), OUT_Y_H_M (0Bh)

Y-axis magnetic data. The value is expressed in 16-bit as two's complement.

8.5 OUT_Z_L_M (0Ch), OUT_Z_H_M (0Dh)

Z-axis magnetic data. The value is expressed in 16-bit as two's complement.

8.6 WHO_AM_I (0Fh)

Table 19. WHO_AM_I register

0	1	0	0	1	0	0	1

Device identification register.

8.7 INT_CTRL_M (12h)

Table 20. INT_CTRL_M register

XMIEN	YMIEN	ZMIEN	PP_OD	IEA	MIEL	4D	MIEN

Table 21. INT_CTRL_M register description

XMIEN	Enable interrupt recognition on X-axis for magnetic data. Default value: 0. (0: disable interrupt recognition; 1: enable interrupt recognition)
YMIEN	Enable interrupt recognition on Y-axis for magnetic data. Default value: 0. (0: disable interrupt recognition; 1: enable interrupt recognition)
ZMIEN	Enable interrupt recognition on Z-axis for magnetic data. Default value: 0. (0: disable interrupt recognition; 1: enable interrupt recognition)
PP_OD	Interrupt pin configuration. Default value: 0. (0: push-pull; 1: open drain)
IEA	Interrupt polarity. Default value: 0. (0: interrupt active-low; 1: interrupt active-high)
MIEL	Latch interrupt request on *INT_SRC_M (13h)* register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched) Once the MIEL is set to '1', the interrupt is cleared by reading the *INT_SRC_M (13h)* register.
4D	4D enable: 4D detection on acceleration data is enabled when 6D bit in *IG_CFG1 (30h)* is set to 1. Default value: 0.
MIEN	Enable interrupt generation for magnetic data. Default value: 0. (0: disable interrupt generation; 1: enable interrupt generation)

8.8 INT_SRC_M (13h)

Table 22. INT_SRC_M register

M_PTH_X	M_PTH_Y	M_PTH_Z	M_NTH_X	M_NTH_Y	M_NTH_Z	MROI	MINT

Table 23. INT_SRC_M register description

M_PTH_X	Magnetic value on X-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Y	Magnetic value on Y-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Z	Magnetic value on Z-axis exceeds the threshold on the positive side. Default value: 0.
M_NTH_X	Magnetic value on X-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Y	Magnetic value on Y-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Z	Magnetic value on Z-axis exceeds the threshold on the negative side. Default value: 0.
MROI	Internal measurement range overflow on magnetic value. Default value: 0.
MINT	Magnetic interrupt event. The magnetic field value exceeds the threshold. Default value: 0.

8.9 INT_THS_L_M (14h), INT_THS_H_M (15h)

Magnetic interrupt threshold. Default value: 0.

The value is expressed in 16-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

Table 24. INT_THS_L_M register

THS7	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 25. INT_THS_H_M register

0	THS14	THS13	THS12	THS11	THS10	THS9	THS8

8.10 OFFSET_X_L_M (16h), OFFSET_X_H_M (17h)

Magnetic offset for X-axis. Default value: 0.

The value is expressed in 16-bit as two's complement.

Table 26. OFFSET_X_L_M register

OFF_X_7	OFF_X_6	OFF_X_5	OFF_X_4	OFF_X_3	OFF_X_2	OFF_X_1	OFF_X_0

Table 27. OFFSET_X_H_M register

OFF_X_15	OFF_X_14	OFF_X_13	OFF_X_12	OFF_X_11	OFF_X_10	OFF_X_9	OFF_X_8

8.11 OFFSET_Y_L_M (18h), OFFSET_Y_H_M (19h)

Magnetic offset for Y-axis. Default value: 0.

The value is expressed in 16-bit as two's complement.

Table 28. OFFSET_Y_L_M register

OFF_Y_7	OFF_Y_6	OFF_Y_5	OFF_Y_4	OFF_Y_3	OFF_Y_2	OFF_Y_1	OFF_Y_0

Table 29. OFFSET_Y_H_M register

OFF_Y_15	OFF_Y_14	OFF_Y_13	OFF_Y_12	OFF_Y_11	OFF_Y_10	OFF_Y_9	OFF_Y_8

8.12 OFFSET_Z_L_M (1Ah), OFFSET_Z_H_M (1Bh)

Magnetic offset for Z-axis. Default value: 0.

The value is expressed in 16-bit as two's complement.

Table 30. OFFSET_Z_L_M register

OFF_Z_7	OFF_Z_6	OFF_Z_5	OFF_Z_4	OFF_Z_3	OFF_Z_2	OFF_Z_1	OFF_Z_0

Table 31. OFFSET_Z_H_M register

OFF_Z_15	OFF_Z_14	OFF_Z_13	OFF_Z_12	OFF_Z_11	OFF_Z_10	OFF_Z_9	OFF_Z_8

8.13 REFERENCE_X (1Ch)

Reference value for high-pass filter for X-axis acceleration data.

8.14 REFERENCE_Y (1Dh)

Reference value for high-pass filter for Y-axis acceleration data.

8.15 REFERENCE_Z (1Eh)

Reference value for high-pass filter for Z-axis acceleration data.

8.16 CTRL0 (1Fh)

Table 32. CTRL0 register

BOOT	FIFO_EN	FTH_EN	0(1)	0(1)	HP_Click	HPIS1	HPIS2

1. These bits must be set to '0' for correct operation of the device.

Table 33. CTRL0 register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
FTH_EN	FIFO programmable threshold enable. Default value: 0 (0: disable; 1: enable)
HP_Click	High-pass filter enabled for click function. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enabled for interrupt generator 1. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for interrupt generator 2. Default value: 0 (0: filter bypassed; 1: filter enabled)

8.17 CTRL1 (20h)

Table 34. CTRL1 register

AODR3	AODR2	AODR1	AODR0	BDU	AZEN	AYEN	AXEN

Table 35. CTRL1 register description

AODR [3:0]	Acceleration data-rate selection. Default value: 0000 (0000: Power-down mode; Others: Refer to *Table 36*)
BDU	Block data update for acceleration and magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
AZEN	Acceleration Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
AYEN	Acceleration Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
AXEN	Acceleration X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

AODR [3:0] is used to set power mode and ODR selection. In the following table bit selection of AODR [3:0] for all frequencies is shown.

Table 36. Acceleration data rate configuration

AODR3	AODR2	AODR1	AODR0	Power mode and ODR selection
0	0	0	0	Power-down mode
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	200 Hz
1	0	0	0	400 Hz
1	0	0	1	800 Hz
1	0	1	0	1600 Hz

8.18 CTRL2 (21h)

Table 37. CTRL2 register

ABW1	ABW0	AFS2	AFS1	AFS0	0(1)	AST	SIM

1. This bit must be set to '0' for correct operation of the device.

Table 38. CTRL2 register description

ABW[1:0]	Accelerometer anti-alias filter bandwidth. Default value: 00 Refer to *Table 39*
AFS[2:0]	Acceleration full-scale selection. Default value: 000 Refer to *Table 40*
AST	Acceleration self-test enable. Default value: 0 (0: self-test disabled; 1: self-test enabled)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Table 39. Acceleration anti-alias filter bandwidth

ABW1	ABW0	Anti-alias filter bandwidth
0	0	773 Hz
0	1	194 Hz

Table 39. Acceleration anti-alias filter bandwidth

ABW1	ABW0	Anti-alias filter bandwidth
1	0	362 Hz
1	1	50 Hz

Table 40. Acceleration full-scale selection

AFS2	AFS1	AFS0	Acceleration full scale
0	0	0	±2 *g*
0	0	1	±4 *g*
0	1	0	±6 *g*
0	1	1	±8 *g*
1	0	0	±16 *g*

8.19 CTRL3 (22h)

Table 41. CTRL3 register

INT1 _BOOT	INT1 _Click	INT1 _IG1	INT1 _IG2	INT1 _IGM	INT1 _DRDY_A	INT1 _DRDY_M	INT1 _EMPTY

Table 42. CTRL3 register description

INT1_BOOT	Boot on INT1 enable. Default value: 0 (0: disable; 1: enable)
INT1_Click	Click generator interrupt on INT1. Default value: 0 (0: disable; 1: enable)
INT1_IG1	Inertial interrupt generator 1 on INT1. Default value: 0 (0: disable; 1: enable)
INT1_IG2	Inertial interrupt generator 2 on INT1. Default value: 0 (0: disable; 1: enable)
INT1_IGM	Magnetic interrupt generator on INT1. Default value: 0 (0: disable; 1: enable)
INT1_DRDY_A	Accelerometer data-ready signal on INT1. Default value: 0 (0: disable; 1: enable)
INT1_DRDY_M	Magnetometer data-ready signal on INT1. Default value: 0 (0: disable; 1: enable)
INT1_EMPTY	FIFO empty indication on INT1. Default value: 0 (0: disable; 1: enable)

8.20 CTRL4 (23h)

Table 43. CTRL4 register

INT2 _Click	INT2 _INT1	INT2 _INT2	INT2 _INTM	INT2 _DRDY_A	INT2 _DRDY_M	INT2 _Overrun	INT2 _FTH

Table 44. CTRL4 register description

INT2 _Click	Click generator interrupt on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _IG1	Inertial interrupt generator 1 on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _IG2	Inertial interrupt generator 2 on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _IGM	Magnetic interrupt generator on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _DRDY_A	Accelerometer data-ready signal on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _DRDY_M	Magnetometer data-ready signal on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _Overrun	FIFO overrun interrupt on INT2. Default value: 0 (0: disable; 1: enable)
INT2 _FTH	FIFO threshold interrupt on INT2. Default value: 0 (0: disable; 1: enable)

8.21 CTRL5 (24h)

Table 45. CTRL5 register

TEMP_EN	M_RES1	M_RES0	M_ODR2	M_ODR1	M_ODR0	LIR2	LIR1

Table 46. CTRL5 register description

TEMP_EN	Temperature sensor enable. Default value: 0 (0: temperature sensor disabled; 1: temperature sensor enabled)
M_RES [1:0]	Magnetic resolution selection. Default value: 00 (00: low resolution, 11: high resolution)
M_ODR [2:0]	Magnetic data rate selection. Default value: 110 Refer to *Table 47*
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)

Table 47. Magnetic data rate configuration

MODR2	MODR1	MODR0	ODR selection
0	0	0	3.125 Hz
0	0	1	6.25 Hz
0	1	0	12.5 Hz
0	1	1	25 Hz
1	0	0	50 Hz
1	0	1	100 Hz(1)
1	1	0	Do not use
1	1	1	Reserved

1. Available only for accelerometer ODR > 50 Hz or accelerometer in power-down mode (refer to *Table 36,* AODR setting).

8.22 CTRL6 (25h)

Table 48. CTRL6 register

0(1)	MFS1	MFS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to '0' for correct operation of the device.

Table 49. CTRL6 register description

MFS [1:0]	Magnetic full-scale selection. Default value: 01 Refer to *Table 50*

Table 50. Magnetic full-scale selection

MFS1	MFS0	Magnetic full scale
0	0	±2 gauss
0	1	±4 gauss
1	0	±8 gauss
1	1	±12 gauss

8.23 CTRL7 (26h)

Table 51. CTRL7 register

AHPM1	AHPM0	AFDS	T_ONLY	0(1)	MLP	MD1	MD0

1. This bit must be set to '0' for correct operation of the device.

Table 52. CTRL7 register description

AHPM[1:0]	High-pass filter mode selection for acceleration data. Default value: 00 Refer to *Table 53*
AFDS	Filtered acceleration data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
T_ONLY	Temperature sensor only mode. Default value: 0 If this bit is set to '1', the temperature sensor is on while the magnetic sensor is off.
MLP	Magnetic data low-power mode. Default value: 0 If this bit is '1', the M_ODR [2:0] is set to 3.125 Hz independently from the MODR settings. Once the bit is set to '0', the magnetic data rate is configured by the MODR bits in the *CTRL5 (24h)* register.
MD[1:0]	Magnetic sensor mode selection. Default 10 Refer to *Table 54*

Table 53. High-pass filter mode selection

AHPM1	AHPM0	High-pass filter mode
0	0	Normal mode (reset X, Y and Z-axis, reading respective *REFERENCE_X (1Ch)*, *REFERENCE_Y (1Dh)* and *REFERENCE_Z (1Eh)* registers)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Auto-reset on interrupt event

Table 54. Magnetic sensor mode selection

MD1	MD0	Magnetic sensor mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Power-down mode
1	1	Power-down mode

8.24 STATUS_A (27h)

Table 55. STATUS_A register

ZYXAOR	ZAOR	YAOR	XAOR	ZYXADA	ZADA	YADA	XADA

Table 56. STATUS_A register description

ZYXAOR	Acceleration X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous data)
ZAOR	Acceleration Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YAOR	Acceleration Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XAOR	Acceleration X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXADA	Acceleration X, Y and Z-axis new value available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZADA	Acceleration Z-axis new value available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YADA	Acceleration Y-axis new value available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XADA	Acceleration X-axis new value available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.25 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data. The value is expressed in 16-bit as two's complement.

8.26 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data. The value is expressed in 16-bit as two's complement.

8.27 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data. The value is expressed in 16-bit as two's complement.

8.28 FIFO_CTRL (2Eh)

Table 57. FIFO_CTRL register

FM2	FM1	FM0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 58. FIFO_CTRL register description

FM[2:0]	FIFO mode selection. Default value: 000 Refer to *Table 59*
FTH[4:0]	FIFO threshold level. Default value: 00000

Table 59. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

Interrupt generator 2 can change the FIFO mode.

8.29 FIFO_SRC (2Fh)

FiFO status register.

Table 60. FIFO_SRC register

FTH	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 61. FIFO_SRC register description

FTH	FIFO threshold status. FTH bit is set to ‘1’ when FIFO content exceeds threshold level.
OVRN	FIFO overrun status. OVRN bit is set to ‘1’ when FIFO buffer is full.
EMPTY	Empty status. EMPTY bit is set to ‘1’ when all FIFO samples have been read and FIFO is empty.
FSS[4:0]	FIFO stored data level. FSS4-0 bits contain the current number of unread FIFO levels.

8.30 IG_CFG1 (30h)

Inertial interrupt generator 1 configuration register.

Table 62. IG_CFG1 register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 63. IG_CFG1 register description

AOI	And/Or combination of interrupt events. Default value: 0. Refer to *Table 64*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 64*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/ XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Content of this register is loaded at boot.

Write operation at this address is possible only after system boot.

Table 64. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

8.31 IG_SRC1 (31h)

Inertial interrupt generator 1 status register.

Table 65. IG_SRC1 register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 66. IG_SRC1 register description

IA	Interrupt status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt; 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt; 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt; 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt; 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt; 1: X low event has occurred)

Reading at this address clears the *IG_SRC1 (31h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *IG_SRC1 (31h)* register if the latched option was chosen.

8.32 IG_THS1 (32h)

Table 67. IG_THS1 register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 68. IG_THS1 register description

THS[6:0]	Interrupt generator 1 threshold. Default value: 000 0000

8.33 IG_DUR1 (33h)

Table 69. IG1_DUR1 register

0	D6	D5	D4	D3	D2	D1	D0

Table 70. IG1_DUR1 register description

D[6:0]	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.34 IG_CFG2 (34h)

This register contains the settings for the inertial interrupt generator 2.

Table 71. IG_CFG2 register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 72. IG_CFG2 register description

AOI	And/Or combination of interrupt events. Default value: 0. Refer to *Table 73*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 73*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/ XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Content of this register is loaded at boot.

Write operation at this address is possible only after system boot.

Table 73. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains until the orientation is inside the zone.

8.35 IG_SRC2 (35h)

This register contains the status for the inertial interrupt generator 2.

Table 74. IG_SRC2 register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 75. IG_SRC2 register description

IA	Interrupt generator 2 status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt; 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt; 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt; 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt; 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt; 1: X low event has occurred)

Reading at this address clears the *IG_SRC2 (35h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refresh of data in the *IG_SRC2 (35h)* register if the latched option was chosen.

8.36 IG_THS2 (36h)

Table 76. IG2_THS2 register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 77. IG2_THS2 register description

THS[6:0]	Interrupt generator 2 threshold. Default value: 000 0000

8.37 IG_DUR2 (37h)

Table 78. IG_DUR2 register

0	D6	D5	D4	D3	D2	D1	D0

Table 79. IG_DUR2 register description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.38 CLICK_CFG (38h)

Table 80. CLICK_CFG register

--	--	ZD	ZS	YD	YS	XD	XS

Table 81. CLICK_CFG register description

ZD	Enable interrupt double-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.39 CLICK_SRC (39h)

Table 82. CLICK_SRC register

--	IA	DClick	SClick	Sign	Z	Y	X

Table 83. CLICK_SRC register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DClick	Double-click enable. Default value: 0 (0: double-click detection disable; 1: double-click detection enable)
SClick	Single-click enable. Default value: 0 (0: single-click detection disable; 1: single-click detection enable)
Sign	Click sign. 0: positive detection; 1: negative detection
Z	Z-click detection. Default value: 0 (0: no interrupt; 1: Z high event has occurred)
Y	Y-click detection. Default value: 0 (0: no interrupt; 1: Y high event has occurred)
X	X-click detection. Default value: 0 (0: no interrupt; 1: X high event has occurred)

8.40 CLICK_THS (3Ah)

Table 84. CLICK_THS register

-	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 85. CLICK_THS register description

Ths[6:0]	Click threshold. Default value: 000 0000

8.41 TIME_LIMIT (3Bh)

Table 86. TIME_LIMIT register

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 87. TIME_LIMIT register description

TLI[6:0]	Click time limit. Default value: 000 0000

8.42 TIME_LATENCY (3Ch)

Table 88. TIME_LATENCY register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 89. TIME_LATENCY register description

TLA[7:0]	Double-click time latency. Default value: 0000 0000

8.43 TIME_WINDOW (3Dh)

Table 90. TIME_WINDOW register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 91. TIME_WINDOW register description

TW[7:0]	Double-click time window

8.44 ACT_THS (3Eh)

Table 92. ACT_THS register

--	ACTH6	ACTH5	ACTH4	ACTH3	ACTH2	ACTH1	ACTH0

Table 93. ACT_THS register description

ACTH[6:0]	Sleep-to-Wake, Return-to-Sleep activation threshold 1 LSb = 16 *mg*

8.45 ACT_DUR (3Fh)

Table 94. ACT_DUR register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 95. ACT_DUR register description

ActD[7:0]	Sleep-to-Wake, Return-to-Sleep duration DUR = (Act_DUR + 1)*8/ODR

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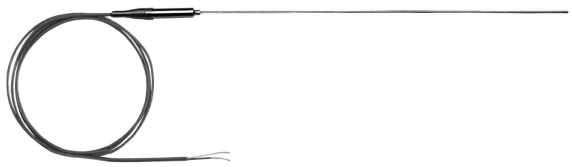
TRANSITION JOINT PROBES AND ACCESSORIES

MODEL TMP - TRANSITION JOINT PROBES



- *CHOICE OF 304 SS, INCONEL 600 OR XL SHEATH*
- *STRIPPED BARE WIRE ENDS*
- *XL HIGH TEMPERATURE PROBE AVAILABLE*
- *EASILY ATTACHES TO STANDARD AND MINI STYLE CONNECTORS (SEE ACCESSORIES)*
- *MEETS OR EXCEEDS SLE AND EN 60584-2: TOLERANCE CLASS 1*

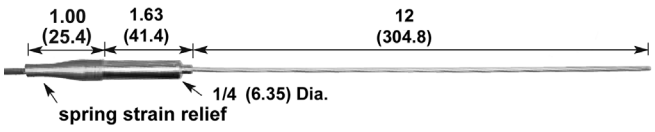
GENERAL DESCRIPTION

Model TMPTJ transition joint probes are rugged temperature probes that feature a spring strain relief at the "cold" end of the probe that prevents pinching of the thermocouple wire that can occur in certain applications. These versatile probes come in a variety of sheath diameters and materials. The probes are standard 12" long transitioning to 40" of wire with exposed leads.

SPECIFICATIONS

1. **SHEATH**: Constructed of 304 stainless steel, Inconel 600, or XL (High Temperature Probe)
2. **SHEATH DIAMETER**: 1/16" or 1/8"
3. **PROBE LENGTH**: 12" Ungrounded junction.
4. **CONNECTOR BODY**: Glass Filled Nylon, rated to 260 ºC.
5. **WIRE INSULATION**: Neoflon PFA
6. **LEAD LENGTH**: 40" (1 meter) with stripped ends

DIMENSIONS In inches (mm)



Note: Probe supplied with 1M (40") cable

ORDERING INFORMATION

DESCRIPTION	ANSI TYPE TC	SHEATH MATERIAL	SHEATH DIAMETER INCHES	UPPER TEMP GUIDELINES °C (°F) TC JUNCTION	PART NUMBER
TRANSITION JOINT PROBES	K	INCONEL 600	1/16	921 (1690)	TMPKTJ01
	K	INCONEL 600	1/8	1071 (1960)	TMPKTJ02
	K	304 SS	1/16	899 (1650)	TMPKTJ03
	K	304 SS	1/8	899 (1650)	TMPKTJ04
	K	XL	1/8	1038 (1900)	TMPKTJ05
	K	XL	1/16	1149 (2100)	TMPKTJ06

** XL probes have a very low drift and are for use in high temperature applications up to 1335 °C.*

Do not dispose of unit in trash - Recycle

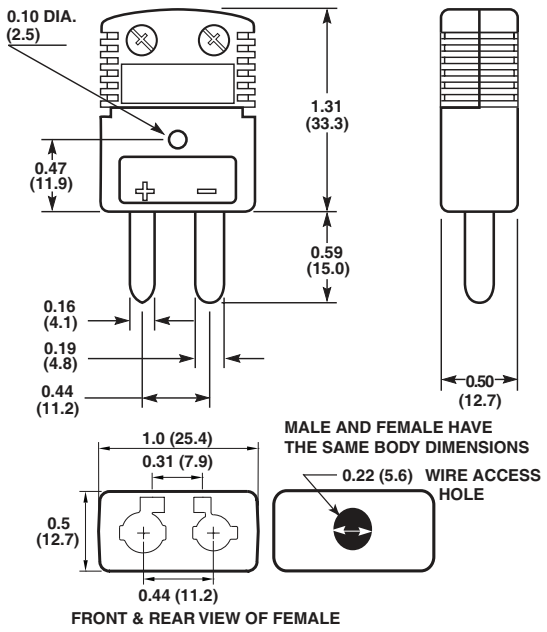
ACCESSORIES

MODEL TMPCN - QUICK DISCONNECT STANDARD CONNECTORS

GENERAL DESCRIPTION

Standard Connectors are for use with the Standard Quick Disconnect TC Probes. They are available in both male and female termination, and include a "write on label" for easy identification. The female standard connector is a universal connector, meaning it can be used to terminate male versions of both the standard and miniature connector.

DIMENSIONS In inches (mm)



SPECIFICATIONS

1. **CONNECTOR BODY MATERIAL**: Glass Filled Nylon, for temperature ranges of -29 to 220º C. (-20 to 428 °F)
2. **CONNECTOR BODY COLOR**: ANSI color coded
3. **WIRE GAGE**: Accepts stranded or solid wire up to 14 AWG
4. **WIRE TERMINATION**: Combination Phillips/Slot Screws

ORDERING INFORMATION

DESCRIPTION	TYPE	TERMINATION	PART NUMBER
STANDARD CONNECTOR	K	MALE	TMPCNS01
		FEMALE	TMPCNS02
	T	MALE	TMPCNS03
		FEMALE	TMPCNS04
	E	MALE	TMPCNS05
		FEMALE	TMPCNS06
	J	MALE	TMPCNS07
		FEMALE	TMPCNS08

Do not dispose of unit in trash - Recycle

MODEL TMPCN - QUICK DISCONNECT MINIATURE CONNECTORS

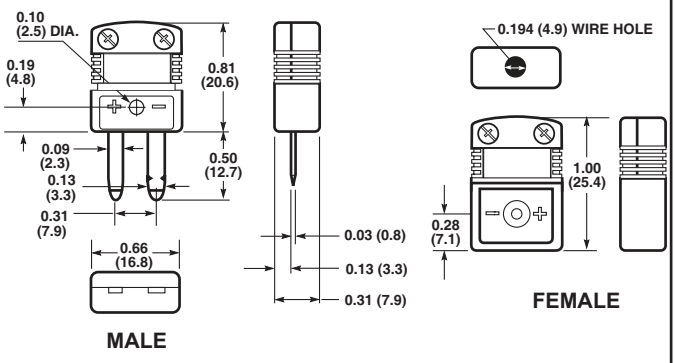
GENERAL DESCRIPTION

Miniature Connectors are for use with the Miniature Quick Disconnect TC Probes. They are available in both male and female termination, and include a "write on label" for easy identification.

SPECIFICATIONS

1. **CONNECTOR BODY MATERIAL**: Glass Filled Nylon, for temperature ranges of -29 to 220º C. (-20 to 428 °F)
2. **CONNECTOR BODY COLOR**: ANSI color coded
3. **WIRE GAGE**: Accepts stranded or solid wire up to 20 AWG
4. **WIRE TERMINATION**: Combination Phillips/Slot Screws

DIMENSIONS In inches (mm)



ORDERING INFORMATION

DESCRIPTION	TYPE	TERMINATION	PART NUMBER
MINIATURE CONNECTOR	K	MALE	TMPCNM01
		FEMALE	TMPCNM02
	T	MALE	TMPCNM03
		FEMALE	TMPCNM04
	E	MALE	TMPCNM05
		FEMALE	TMPCNM06
	J	MALE	TMPCNM07
		FEMALE	TMPCNM08

Do not dispose of unit in trash - Recycle

28.1 ADC12_A Introduction

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator (MSP430F54xx (non-A only) – in other devices, separate REF module), and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent analog-to-digital converter (ADC) samples to be converted and stored without any CPU intervention.

ADC12_A features include:

- Greater than 200-ksps maximum conversion rate
- Monotonic 12-bit converter with no missing codes
- Sample-and-hold with programmable sampling periods controlled by software or timers
- Conversion initiation by software or timers
- Software-selectable on-chip reference voltage generation (MSP430F54xx (non-A only): 1.5 V or 2.5 V, all other devices: 1.5 V, 2.0 V, or 2.5 V)
- Software-selectable internal or external reference
- Up to 12 individually configurable external input channels
- Conversion channels for internal temperature sensor, AV_{CC}, and external references
- Independent channel-selectable reference sources for both positive and negative references
- Selectable conversion clock source
- Single-channel, repeat-single-channel, sequence (autoscan), and repeat-sequence (repeated autoscan) conversion modes
- ADC core and reference voltage can be powered down separately
- Interrupt vector register for fast decoding of 18 ADC interrupts
- 16 conversion-result storage registers

The block diagram of ADC12_A is shown in Figure 28-1. In MSP430F54xx (non-A only), the reference generator is located in the ADC12_A module itself. In other devices, the reference generator is located in the reference module, REF. See the REF module chapter and the device-specific data sheet for further details. Figure 28-1 shows the block diagram for devices that have the REF module available. Figure 28-2 shows the block diagram for the MSP430F54xx (non-A only) which does not incorporate the REF module.

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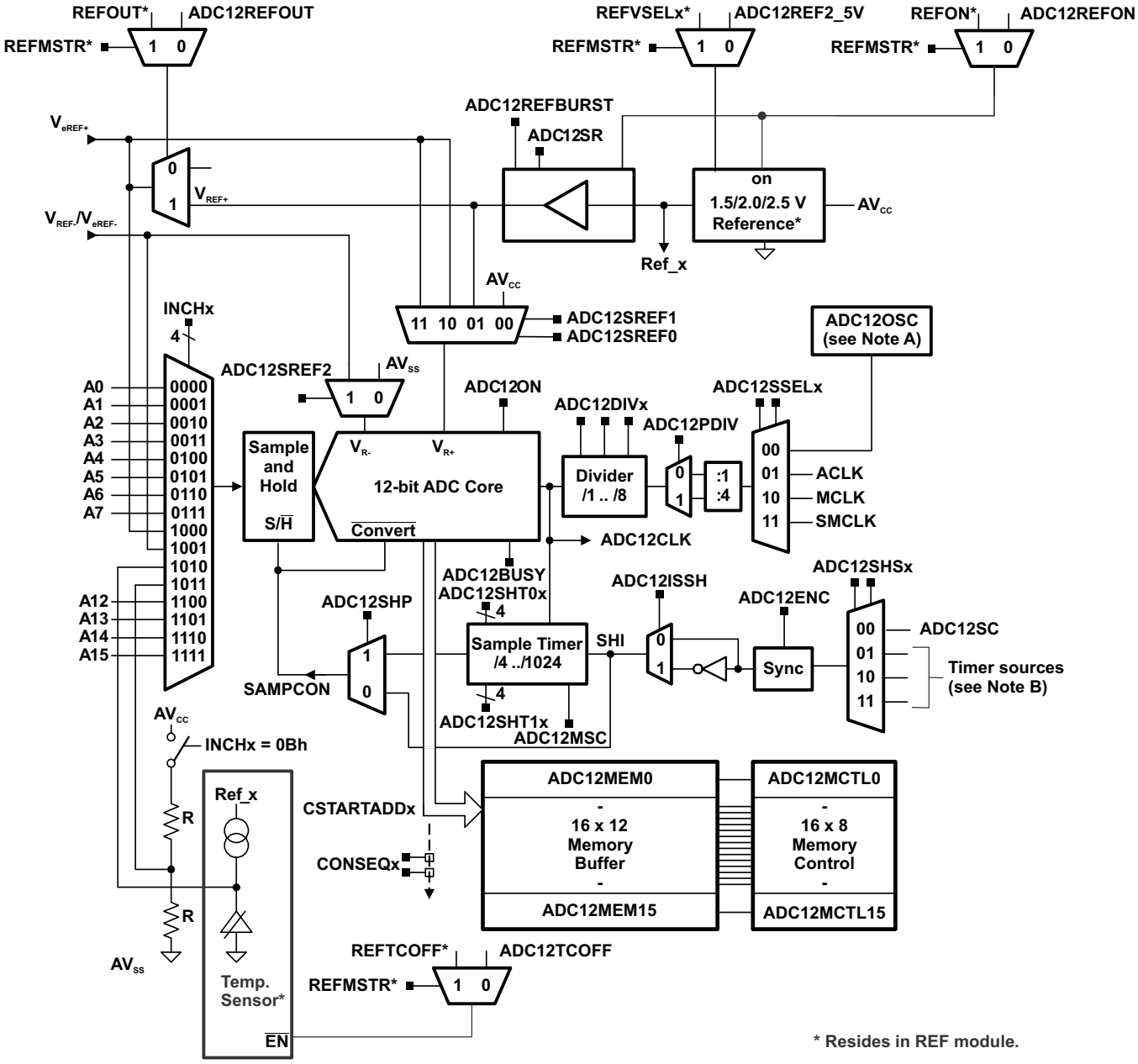

A ADC12OSC refers to the MODCLK from the UCS. See the UCS chapter for more information.

B See the device-specific data sheet for timer sources available.

Figure 28-1. ADC12_A Block Diagram (Devices With REF Module)

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28.2 ADC12_A Operation

The ADC12_A module is configured with user software. The setup and operation of the ADC12_A is discussed in the following sections.

28.2.1 12-Bit ADC Core

The ADC core converts an analog input to its 12-bit digital representation and stores the result in conversion memory. The core uses two programmable and selectable voltage levels (V_{R+} and V_{R-}) to define the upper and lower limits of the conversion. The digital output (N_{ADC}) is full scale (0FFFh) when the input signal is equal to or higher than V_{R+}. The digital output (N_{ADC}) is zero when the input signal is equal to or lower than V_{R-}. The input channel and the reference voltage levels (V_{R+} and V_{R-}) are defined in the conversion-control memory. The conversion formula for the ADC result N_{ADC} is:

$$N_{ADC} = 4095 \times \frac{Vin - V_{R-}}{V_{R+} - V_{R-}}$$

The ADC12_A core is configured by two control registers, ADC12CTL0 and ADC12CTL1. The core is enabled with the ADC12ON bit. The ADC12_A can be turned off when it is not in use to save power. With few exceptions, the ADC12_A control bits can be modified only when ADC12ENC = 0. ADC12ENC must be set to 1 before any conversion can take place.

28.2.1.1 Conversion Clock Selection

The ADC12CLK is used both as the conversion clock and to generate the sampling period when the pulse sampling mode is selected. The ADC12_A source clock is selected using the predivider controlled by the ADC12PDIV bit and the divider using the ADC12SSELx bits. The input clock can be divided from 1 to 32 using both the ADC12DIVx bits and the ADC12PDIV bit. Possible ADC12CLK sources are SMCLK, MCLK, ACLK, and the ADC12OSC.

The ADC12OSC in the block diagram (see Figure 28-1) refers to the MODCLK 5-MHz oscillator from the UCS (see the UCS module for more information) which can vary with individual devices, supply voltage, and temperature. See the device-specific data sheet for the ADC12OSC specification.

The user must ensure that the clock chosen for ADC12CLK remains active until the end of a conversion. If the clock is removed during a conversion, the operation does not complete and the results are invalid.

28.2.2 ADC12_A Inputs and Multiplexer

The 12 external and 4 internal analog signals are selected as the channel for conversion by the analog input multiplexer. The input multiplexer is a break-before-make type to reduce input-to-input noise injection resulting from channel switching (see Figure 28-3). The input multiplexer is also a T-switch to minimize the coupling between channels. Channels that are not selected are isolated from the ADC, and the intermediate node is connected to analog ground (AV_{SS}) so that the stray capacitance is grounded to eliminate crosstalk.

The ADC12_A uses the charge redistribution method. When the inputs are internally switched, the switching action may cause transients on the input signal. These transients decay and settle before causing errant conversion.

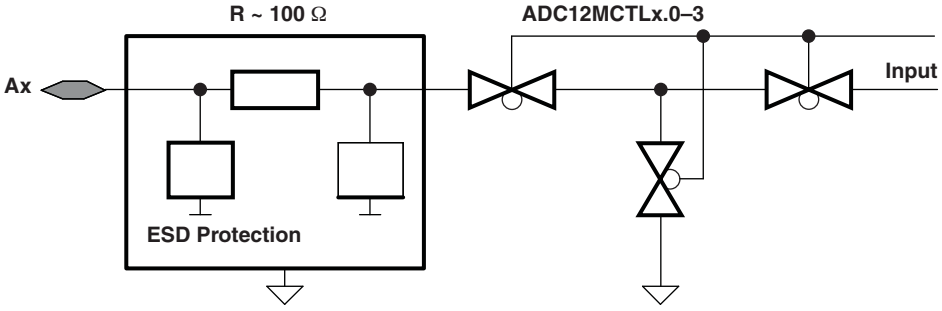

Figure 28-3. Analog Multiplexer

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The internal reference buffer also has selectable speed versus power settings. When the maximum conversion rate is below 50 ksps, setting ADC12SR = 1 reduces the current consumption of the buffer by approximately 50%.

28.2.4 Auto Power Down

The ADC12_A is designed for low-power applications. When the ADC12_A is not actively converting, the core is automatically disabled, and it is automatically reenabled when needed. The MODOSC is also automatically enabled when needed and disabled when not needed.

28.2.5 Sample and Conversion Timing

An analog-to-digital conversion is initiated with a rising edge of the sample input signal SHI. The source for SHI is selected with the SHSx bits and includes the following:

- ADC12SC bit
- Up to three timer outputs (see the device-specific data sheet for available timer sources)

The ADC12_A supports 8-bit, 10-bit, and 12-bit resolution modes selectable by the ADC12RES bits. The analog-to-digital conversion requires 9, 11, and 13 ADC12CLK cycles, respectively. The polarity of the SHI signal source can be inverted with the ADC12ISSH bit. The SAMPCON signal controls the sample period and start of conversion. When SAMPCON is high, sampling is active. The high-to-low SAMPCON transition starts the analog-to-digital conversion. Two different sample-timing methods are defined by control bit ADC12SHP, extended sample mode and pulse mode. See the device-specific data sheet for available timers for SHI sources.

28.2.5.1 Extended Sample Mode

The extended sample mode is selected when ADC12SHP = 0. The SHI signal directly controls SAMPCON and defines the length of the sample period t_{sample}. When SAMPCON is high, sampling is active. The high-to-low SAMPCON transition starts the conversion after synchronization with ADC12CLK (see Figure 28-4).

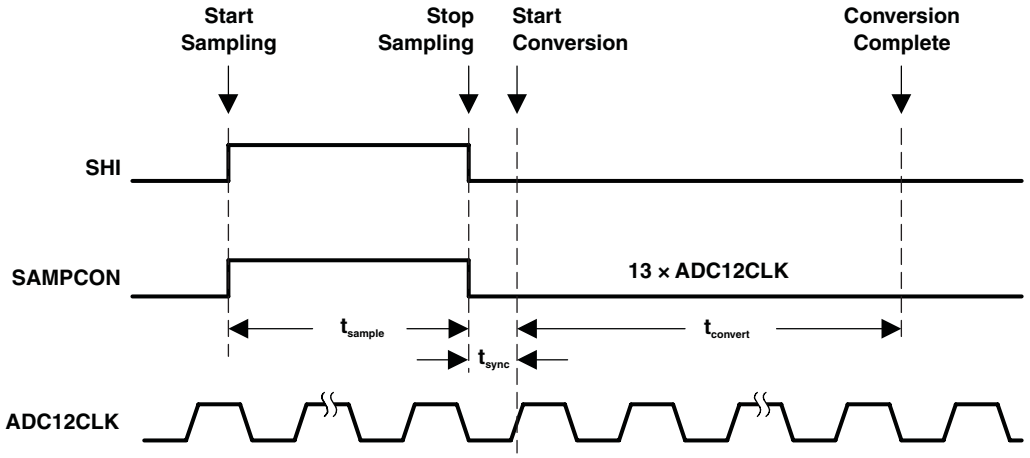

Figure 28-4. Extended Sample Mode

28.2.5.2 Pulse Sample Mode

Set ADC12SHP = 1 to select the pulse sample mode. The SHI signal is used to trigger the sampling timer. The ADC12SHT0x and ADC12SHT1x bits in ADC12CTL0 control the interval of the sampling timer that defines the SAMPCON sample period t_{sample}. The sampling timer keeps SAMPCON high after synchronization with AD12CLK for a programmed interval t_{sample}. The total sampling time is t_{sample} plus t_{sync} (see Figure 28-5).

The ADC12SHTx bits select the sampling time in 4× multiples of ADC12CLK. ADC12SHT0x selects the sampling time for ADC12MCTL0 to ADC12MCTL7. ADC12SHT1x selects the sampling time for ADC12MCTL8 to ADC12MCTL15.

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28.2.10 ADC12_A Interrupts

The ADC12_A has 18 interrupt sources:

- ADC12IFG0 to ADC12IFG15
- ADC12OV, ADC12MEMx overflow
- ADC12TOV, ADC12_A conversion time overflow

The ADC12IFGx bits are set when their corresponding ADC12MEMx memory register is loaded with a conversion result. An interrupt request is generated if the corresponding ADC12IEx bit and the GIE bit are set. The ADC12OV condition occurs when a conversion result is written to any ADC12MEMx before its previous conversion result was read. The ADC12TOV condition is generated when another sample-and-conversion is requested before the current conversion is completed. The DMA is triggered after the conversion in single-channel conversion mode or after the completion of a sequence of channel conversions in sequence-of-channels conversion mode.

28.2.10.1 ADC12IV, Interrupt Vector Generator

All ADC12_A interrupt sources are prioritized and combined to source a single interrupt vector. The interrupt vector register ADC12IV is used to determine which enabled ADC12_A interrupt source requested an interrupt.

The highest-priority enabled ADC12_A interrupt generates a number in the ADC12IV register (see register description). This number can be evaluated or added to the program counter (PC) to automatically enter the appropriate software routine. Disabled ADC12_A interrupts do not affect the ADC12IV value.

Any access, read or write, of the ADC12IV register automatically resets the ADC12OV condition or the ADC12TOV condition if either was the highest-pending interrupt. Neither interrupt condition has an accessible interrupt flag. The ADC12IFGx flags are not reset by an ADC12IV access. ADC12IFGx bits are reset automatically by accessing their associated ADC12MEMx register or may be reset with software.

If another interrupt is pending after servicing of an interrupt, another interrupt is generated. For example, if the ADC12OV and ADC12IFG3 interrupts are pending when the interrupt service routine accesses the ADC12IV register, the ADC12OV interrupt condition is reset automatically. After the RETI instruction of the interrupt service routine is executed, the ADC12IFG3 generates another interrupt.

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28.3.1 ADC12CTL0 Register

ADC12_A Control Register 0

Figure 28-13. ADC12CTL0 Register

15	14	13	12	11	10	9	8
ADC12SHT1x				ADC12SHT0x			
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC12MSC	ADC12REF2_5V	ADC12REFON	ADC12ON	ADC12OVIE	ADC12TOVIE	ADC12ENC	ADC12SC
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ADC12ENC = 0

Table 28-4. ADC12CTL0 Register Description

Bit	Field	Type	Reset	Description
15-12	ADC12SHT1x	RW	0h	ADC12_A sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM8 to ADC12MEM15.
11-8	ADC12SHT0x	RW	0h	ADC12_A sample-and-hold time. These bits define the number of ADC12CLK cycles in the sampling period for registers ADC12MEM0 to ADC12MEM7. 0000b = 4 ADC12CLK cycles 0001b = 8 ADC12CLK cycles 0010b = 16 ADC12CLK cycles 0011b = 32 ADC12CLK cycles 0100b = 64 ADC12CLK cycles 0101b = 96 ADC12CLK cycles 0110b = 128 ADC12CLK cycles 0111b = 192 ADC12CLK cycles 1000b = 256 ADC12CLK cycles 1001b = 384 ADC12CLK cycles 1010b = 512 ADC12CLK cycles 1011b = 768 ADC12CLK cycles 1100b = 1024 ADC12CLK cycles 1101b = 1024 ADC12CLK cycles 1110b = 1024 ADC12CLK cycles 1111b = 1024 ADC12CLK cycles
7	ADC12MSC	RW	0h	ADC12_A multiple sample and conversion. Valid only for sequence or repeated modes. 0b = The sampling timer requires a rising edge of the SHI signal to trigger each sample-and-convert. 1b = The first rising edge of the SHI signal triggers the sampling timer, but further sample-and-conversions are performed automatically as soon as the prior conversion is completed.
6	ADC12REF2_5V	RW	0h	ADC12_A reference generator voltage. ADC12REFON must also be set. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = 1.5 V 1b = 2.5 V
5	ADC12REFON	RW	0h	ADC12_A reference generator on. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = Reference off 1b = Reference on
4	ADC12ON	RW	0h	ADC12_A on 0b = ADC12_A off 1b = ADC12_A on

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Table 28-4. ADC12CTL0 Register Description (continued)

Bit	Field	Type	Reset	Description
3	ADC12OVIE	RW	0h	ADC12MEMx overflow-interrupt enable. The GIE bit must also be set to enable the interrupt. 0b = Overflow interrupt disabled 1b = Overflow interrupt enabled
2	ADC12TOVIE	RW	0h	ADC12_A conversion-time-overflow interrupt enable. The GIE bit must also be set to enable the interrupt. 0b = Conversion time overflow interrupt disabled 1b = Conversion time overflow interrupt enabled
1	ADC12ENC	RW	0h	ADC12_A enable conversion 0b = ADC12_A disabled 1b = ADC12_A enabled
0	ADC12SC	RW	0h	ADC12_A start conversion. Software-controlled sample-and-conversion start. ADC12SC and ADC12ENC may be set together with one instruction. ADC12SC is reset automatically. 0b = No sample-and-conversion-start 1b = Start sample-and-conversion

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28.3.2 ADC12CTL1 Register

ADC12_A Control Register 1

Figure 28-14. ADC12CTL1 Register

15	14	13	12	11	10	9	8
ADC12CSTARTADDx				ADC12SHSx		ADC12SHP	ADC12ISSH
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC12DIVx			ADC12SSELx		ADC12CONSEQx		ADC12BUSY
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-(0)

Can be modified only when ADC12ENC = 0

Table 28-5. ADC12CTL1 Register Description

Bit	Field	Type	Reset	Description
15-12	ADC12CSTARTADDx	RW	0h	ADC12_A conversion start address. These bits select which ADC12_A conversion-memory register is used for a single conversion or for the first conversion in a sequence. The value of CSTARTADDx is 0 to 0Fh, corresponding to ADC12MEM0 to ADC12MEM15.
11-10	ADC12SHSx	RW	0h	ADC12_A sample-and-hold source select 00b = ADC12SC bit 01b = Timer source (see device-specific data sheet for exact timer and locations) 10b = Timer source (see device-specific data sheet for exact timer and locations) 11b = Timer source (see device-specific data sheet for exact timer and locations)
9	ADC12SHP	RW	0h	ADC12_A sample-and-hold pulse-mode select. This bit selects the source of the sampling signal (SAMPCON) to be either the output of the sampling timer or the sample-input signal directly. 0b = SAMPCON signal is sourced from the sample-input signal. 1b = SAMPCON signal is sourced from the sampling timer.
8	ADC12ISSH	RW	0h	ADC12_A invert signal sample-and-hold 0b = The sample-input signal is not inverted. 1b = The sample-input signal is inverted.
7-5	ADC12DIVx	RW	0h	ADC12_A clock divider 000b = Divide by 1 001b = Divide by 2 010b = Divide by 3 011b = Divide by 4 100b = Divide by 5 101b = Divide by 6 110b = Divide by 7 111b = Divide by 8
4-3	ADC12SSELx	RW	0h	ADC12_A clock source select 00b = ADC12OSC (MODCLK) 01b = ACLK 10b = MCLK 11b = SMCLK
2-1	ADC12CONSEQx	RW	0h	ADC12_A conversion sequence mode select 00b = Single-channel, single-conversion 01b = Sequence-of-channels 10b = Repeat-single-channel 11b = Repeat-sequence-of-channels
0	ADC12BUSY	R	0h	ADC12_A busy. This bit indicates an active sample or conversion operation. 0b = No operation is active. 1b = A sequence, sample, or conversion is active.

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28.3.3 ADC12CTL2 Register

ADC12_A Control Register 2

Figure 28-15. ADC12CTL2 Register

15	14	13	12	11	10	9	8
Reserved							ADC12PDIV
r-0	r-0	r-0	r-0	r-0	r-0	r-0	rw-0
7	6	5	4	3	2	1	0
ADC12TCOFF	Reserved	ADC12RES		ADC12DF	ADC12SR	ADC12REFOUT	ADC12REFBURST
rw-(0)	r-0	rw-(1)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Can be modified only when ADC12ENC = 0

Table 28-6. ADC12CTL2 Register Description

Bit	Field	Type	Reset	Description
15-9	Reserved	R	0h	Reserved. Always reads as 0.
8	ADC12PDIV	RW	0h	ADC12_A predivider. This bit predivides the selected ADC12_A clock source. 0b = Predivide by 1 1b = Predivide by 4
7	ADC12TCOFF	RW	0h	ADC12_A temperature sensor off. If the bit is set, the temperature sensor turned off. This is used to save power. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = Temperature sensor on 1b = Temperature sensor off
6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	ADC12RES	RW	2h	ADC12_A resolution. This bit defines the conversion result resolution. 00b = 8 bit (9 clock cycle conversion time) 01b = 10 bit (11 clock cycle conversion time) 10b = 12 bit (13 clock cycle conversion time) 11b = Reserved
3	ADC12DF	RW	0h	ADC12_A data read-back format. Data is always stored in the binary unsigned format. 0b = Binary unsigned. Theoretically, the analog input voltage -VREF results in 0000h, the analog input voltage +VREF results in 0FFFh. 1b = Signed binary (twos complement), left aligned. Theoretically, the analog input voltage -VREF results in 8000h, the analog input voltage +VREF results in 7FF0h.
2	ADC12SR	RW	0h	ADC12_A sampling rate. This bit selects the reference buffer drive capability for the maximum sampling rate. Setting ADC12SR reduces the current consumption of the reference buffer. 0b = Reference buffer supports up to approximately 200 ksps. 1b = Reference buffer supports up to approximately 50 ksps.
1	ADC12REFOUT	RW	0h	Reference output. In devices with the REF module, this bit is only valid if the REFMSTR bit of the REF module is set to 0. In the F54xx devices (non-A), the REF module is not available. 0b = Reference output off 1b = Reference output on
0	ADC12REFBURST	RW	0h	Reference burst 0b = Reference buffer on continuously 1b = Reference buffer on only during sample-and-conversion

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28.3.4 ADC12MEMx Register

ADC12_A Conversion Memory Register

Figure 28-16. ADC12MEMx Register

15	14	13	12	11	10	9	8
Conversion Results							
rw	rw	rw	rw	rw	rw	rw	rw
7	6	5	4	3	2	1	0
Conversion Results							
rw	rw	rw	rw	rw	rw	rw	rw

Table 28-7. ADC12MEMx Register Description

Bit	Field	Type	Reset	Description
15-0	Conversion Results	RW	undefined	Binary unsigned format: This data format is used if ADC12DF = 0. The 12-bit conversion results are right justified. Bit 11 is the MSB. Bits 15–12 are 0 in 12-bit mode, bits 15–10 are 0 in 10-bit mode, and bits 15–8 are 0 in 8-bit mode. Writing to the conversion memory registers corrupts the results. Twos-complement format: This data format is used if ADC12DF = 1. The 12-bit conversion results are left justified, twos-complement format. Bit 15 is the MSB. Bits 3–0 are 0 in 12-bit mode, bits 5–0 are 0 in 10-bit mode, and bits 7–0 are 0 in 8-bit mode. The data is stored in the right-justified format and is converted to the left-justified twos-complement format during read back.

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28.3.5 ADC12MCTLx Register

ADC12_A Conversion Memory Control Register

Figure 28-17. ADC12MCTLx Register

7	6	5	4	3	2	1	0
ADC12EOS	ADC12SREFx			ADC12INCHx			
rw	rw	rw	rw	rw	rw	rw	rw

Can be modified only when ADC12ENC = 0

Table 28-8. ADC12MCTLx Register Description

Bit	Field	Type	Reset	Description
7	ADC12EOS	RW	0h	End of sequence. Indicates the last conversion in a sequence. 0b = Not end of sequence 1b = End of sequence
6-4	ADC12SREFx	RW	0h	Select reference 000b = V(R+) = AVCC and V(R-) = AVSS 001b = V(R+) = VREF+ and V(R-) = AVSS 010b = V(R+) = VeREF+ and V(R-) = AVSS 011b = V(R+) = VeREF+ and V(R-) = AVSS 100b = V(R+) = AVCC and V(R-) = VREF-/VeREF- 101b = V(R+) = VREF+ and V(R-) = VREF-/VeREF- 110b = V(R+) = VeREF+ and V(R-) = VREF-/VeREF- 111b = V(R+) = VeREF+ and V(R-) = VREF-/VeREF-
3-0	ADC12INCHx	RW	0h	Input channel select 0000b = A0 0001b = A1 0010b = A2 0011b = A3 0100b = A4 0101b = A5 0110b = A6 0111b = A7 1000b = VeREF+ 1001b = VREF-/VeREF- 1010b = Temperature diode 1011b = (AVCC – AVSS) / 2 1100b = A12. On devices with the Battery Backup System, VBAT can be measured internally by the ADC. 1101b = A13 1110b = A14 1111b = A15

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28.3.6 ADC12IE Register

ADC12_A Interrupt Enable Register

Figure 28-18. ADC12IE Register

15	14	13	12	11	10	9	8
ADC12IE15	ADC12IE14	ADC12IE13	ADC12IE12	ADC12IE11	ADC12IE10	ADC12IE9	ADC12IE8
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC12IE7	ADC12IE6	ADC12IE5	ADC12IE4	ADC12IE3	ADC12IE2	ADC12IE1	ADC12IE0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Table 28-9. ADC12IE Register Description

Bit	Field	Type	Reset	Description
15	ADC12IE15	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG15 bit. 0b = Interrupt disabled 1b = Interrupt enabled
14	ADC12IE14	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG14 bit. 0b = Interrupt disabled 1b = Interrupt enabled
13	ADC12IE13	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG13 bit. 0b = Interrupt disabled 1b = Interrupt enabled
12	ADC12IE12	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG12 bit. 0b = Interrupt disabled 1b = Interrupt enabled
11	ADC12IE11	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG11 bit. 0b = Interrupt disabled 1b = Interrupt enabled
10	ADC12IE10	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG10 bit. 0b = Interrupt disabled 1b = Interrupt enabled
9	ADC12IE9	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG9 bit. 0b = Interrupt disabled 1b = Interrupt enabled
8	ADC12IE8	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG8 bit. 0b = Interrupt disabled 1b = Interrupt enabled
7	ADC12IE7	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG7 bit. 0b = Interrupt disabled 1b = Interrupt enabled
6	ADC12IE6	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG6 bit. 0b = Interrupt disabled 1b = Interrupt enabled

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Table 28-9. ADC12IE Register Description (continued)

Bit	Field	Type	Reset	Description
5	ADC12IE5	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG5 bit. 0b = Interrupt disabled 1b = Interrupt enabled
4	ADC12IE4	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG4 bit. 0b = Interrupt disabled 1b = Interrupt enabled
3	ADC12IE3	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG3 bit. 0b = Interrupt disabled 1b = Interrupt enabled
2	ADC12IE2	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG2 bit. 0b = Interrupt disabled 1b = Interrupt enabled
1	ADC12IE1	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG1 bit. 0b = Interrupt disabled 1b = Interrupt enabled
0	ADC12IE0	RW	0h	Interrupt enable. This bit enables or disables the interrupt request for the ADC12IFG0 bit. 0b = Interrupt disabled 1b = Interrupt enabled

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28.3.7 ADC12IFG Register

ADC12_A Interrupt Flag Register

Figure 28-19. ADC12IFG Register

15	14	13	12	11	10	9	8
ADC12IFG15	ADC12IFG14	ADC12IFG13	ADC12IFG12	ADC12IFG11	ADC12IFG10	ADC12IFG9	ADC12IFG8
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)
7	6	5	4	3	2	1	0
ADC12IFG7	ADC12IFG6	ADC12IFG5	ADC12IFG4	ADC12IFG3	ADC12IFG2	ADC12IFG1	ADC12IFG0
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Table 28-10. ADC12IFG Register Description

Bit	Field	Type	Reset	Description
15	ADC12IFG15	RW	0h	ADC12MEM15 interrupt flag. This bit is set when ADC12MEM15 is loaded with a conversion result. This bit is reset if the ADC12MEM15 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
14	ADC12IFG14	RW	0h	ADC12MEM14 interrupt flag. This bit is set when ADC12MEM14 is loaded with a conversion result. This bit is reset if the ADC12MEM14 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
13	ADC12IFG13	RW	0h	ADC12MEM13 interrupt flag. This bit is set when ADC12MEM13 is loaded with a conversion result. This bit is reset if the ADC12MEM13 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
12	ADC12IFG12	RW	0h	ADC12MEM12 interrupt flag. This bit is set when ADC12MEM12 is loaded with a conversion result. This bit is reset if the ADC12MEM12 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
11	ADC12IFG11	RW	0h	ADC12MEM11 interrupt flag. This bit is set when ADC12MEM11 is loaded with a conversion result. This bit is reset if the ADC12MEM11 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
10	ADC12IFG10	RW	0h	ADC12MEM10 interrupt flag. This bit is set when ADC12MEM10 is loaded with a conversion result. This bit is reset if the ADC12MEM10 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
9	ADC12IFG9	RW	0h	ADC12MEM9 interrupt flag. This bit is set when ADC12MEM9 is loaded with a conversion result. This bit is reset if the ADC12MEM9 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending
8	ADC12IFG8	RW	0h	ADC12MEM8 interrupt flag. This bit is set when ADC12MEM8 is loaded with a conversion result. This bit is reset if the ADC12MEM8 is accessed, or it may be reset with software. 0b = No interrupt pending 1b = Interrupt pending

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MSP430F543xA, MSP430F541xA Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Low Supply Voltage Range:
  3.6 V Down to 1.8 V
- Ultra-Low Power Consumption
  - Active Mode (AM):
    All System Clocks Active
    230 µA/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical)
    110 µA/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3):
    Real-Time Clock (RTC) With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
    1.7 µA at 2.2 V, 2.1 µA at 3.0 V (Typical)
    Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wakeup:
    1.2 µA at 3.0 V (Typical)
  - Off Mode (LPM4):
    Full RAM Retention, Supply Supervisor Operational, Fast Wakeup:
    1.2 µA at 3.0 V (Typical)
  - Shutdown Mode (LPM4.5):
    0.1 µA at 3.0 V (Typical)
- Wake up From Standby Mode in 3.5 µs (Typical)
- 16-Bit RISC Architecture
  - Extended Memory
  - Up to 25-MHz System Clock
- Flexible Power-Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Crystals
  - High-Frequency Crystals up to 32 MHz
- 16-Bit Timer TA0, Timer_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer_B With Seven Capture/Compare Shadow Registers
- Up to Four Universal Serial Communication Interfaces
  - USCI_A0, USCI_A1, USCI_A2, and USCI_A3 Each Support:
    - Enhanced UART Supports Automatic Baud-Rate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI_B0, USCI_B1, USCI_B2, and USCI_B3 Each Support:
    - I^2C
    - Synchronous SPI
- 12-Bit Analog-to-Digital Converter (ADC)
  - Internal Reference
  - Sample-and-Hold
  - Autoscan Feature
  - 14 External Channels, 2 Internal Channels
- Hardware Multiplier Supports 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three-Channel Internal DMA
- Basic Timer With RTC Feature
- Section 3 Summarizes the Available Family Members
- For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208)

1.2 Applications

- Analog and Digital Sensor Systems
- Digital Motor Controls
- Remote Controls
- Thermostats
- Digital Timers
- Hand-Held Meters

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

1.3 Description

The TI MSP430™ family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5 µs (typical).

The MSP430F543xA and MSP430F541xA series are microcontroller configurations with three 16-bit timers, a high-performance 12-bit ADC, up to four universal serial communication interfaces (USCIs), a hardware multiplier, DMA, an RTC module with alarm capabilities, and up to 87 I/O pins.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, and hand-held meters.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE(2)
MSP430F5438AZQW	MicroStar Junior™ BGA (113)	7 mm × 7 mm
MSP430F5438APZ	LQFP (100)	14 mm × 14 mm
MSP430F5437APN	LQFP (80)	12 mm × 12 mm

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 8.

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1.4 Functional Block Diagrams

Figure 1-1 and Figure 1-2 show the functional block diagrams.

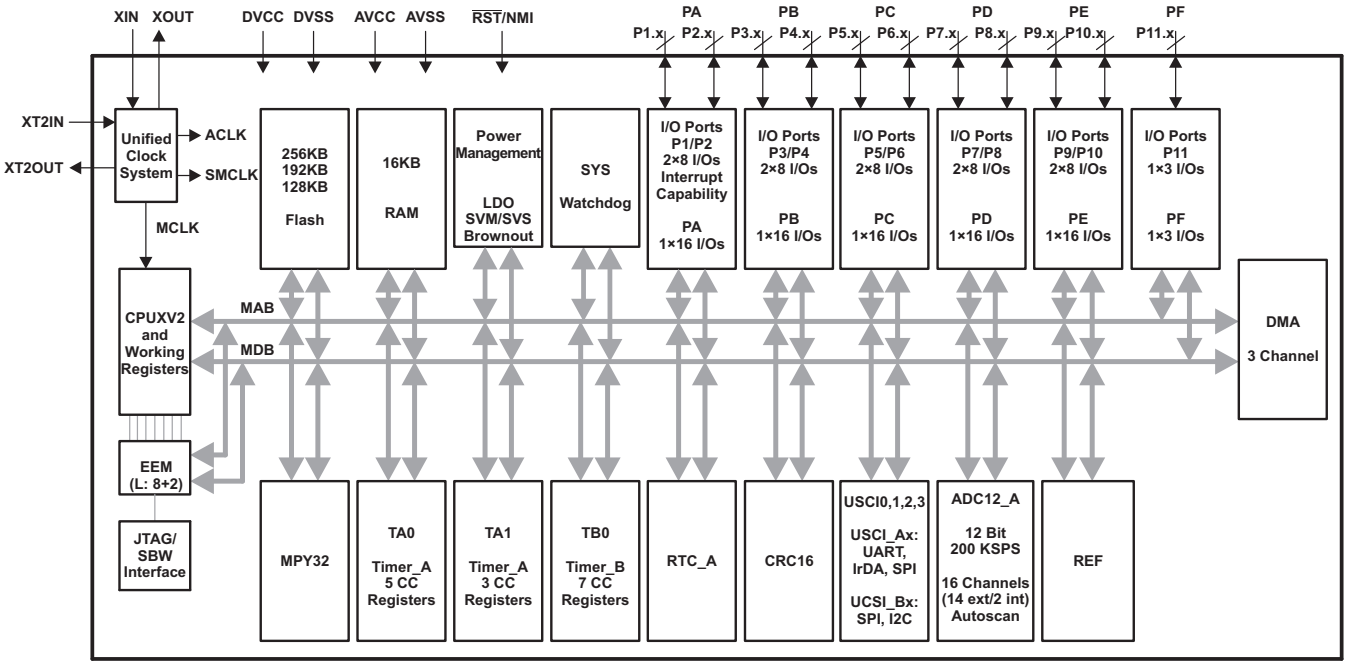

Figure 1-1. Functional Block Diagram – MSP430F5438AIPZ, MSP430F5436AIPZ, MSP430F5419AIPZ, MSP430F5438AIZQW, MSP430F5436AIZQW, MSP430F5419AIZQW

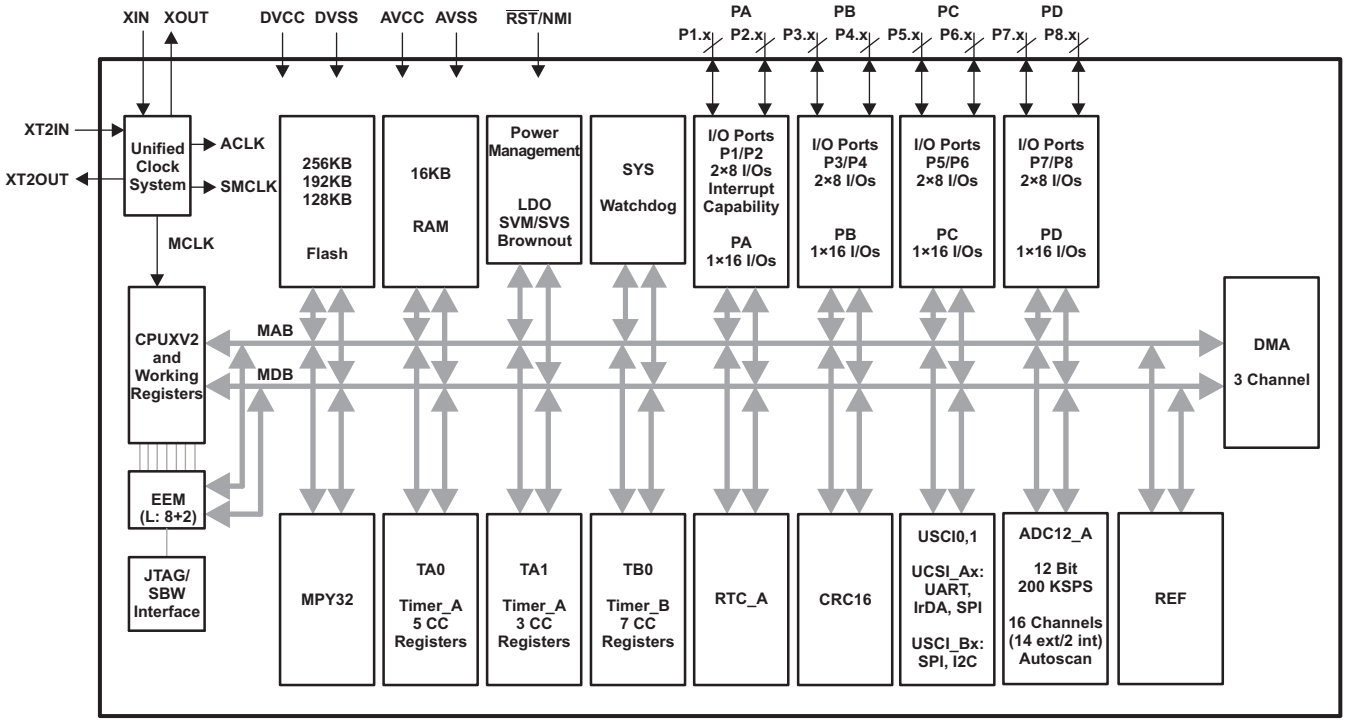

Figure 1-2. Functional Block Diagram – MSP430F5437AIPN, MSP430F5435AIPN, MSP430F5418AIPN

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3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Family Members(1)(2)

DEVICE	FLASH (KB)	SRAM (KB)	Timer_A(3)	Timer_B(4)	USCI		ADC12_A (Ch)	I/O	PACKAGE
					CHANNEL A: UART, IrDA, SPI	CHANNEL B: SPI, I^2C			
MSP430F5438A	256	16	5, 3	7	4	4	14 ext, 2 int	87	100 PZ, 113 ZQW
MSP430F5437A	256	16	5, 3	7	2	2	14 ext, 2 int	67	80 PN
MSP430F5436A	192	16	5, 3	7	4	4	14 ext, 2 int	87	100 PZ, 113 ZQW
MSP430F5435A	192	16	5, 3	7	2	2	14 ext, 2 int	67	80 PN
MSP430F5419A	128	16	5, 3	7	4	4	14 ext, 2 int	87	100 PZ, 113 ZQW
MSP430F5418A	128	16	5, 3	7	2	2	14 ext, 2 int	67	80 PN

(1) For the most current part, package, and ordering information, see the *Package Option Addendum* in Section 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators.

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
Voltage applied to any pin (excluding VCORE)(2)	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Storage temperature, T_{stg} (3)	–55	105	°C
Maximum junction temperature, T_J		95	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (AV_{CC} = $DV_{CC1/2/3/4}$ = DV_{CC})(1)(2)		1.8		3.6	V
V_{SS}	Supply voltage (AV_{SS} = $DV_{SS1/2/3/4}$ = DV_{SS})			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{VCORE}	Recommended capacitor at VCORE(3)			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(4) (5) (see Figure 5-1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V	0		8	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0		12	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		20	
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		25	

(1) TI recommends powering AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Section 5.23 threshold parameters for the exact values and further details.
(3) A capacitor tolerance of ±20% or better is required.
(4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

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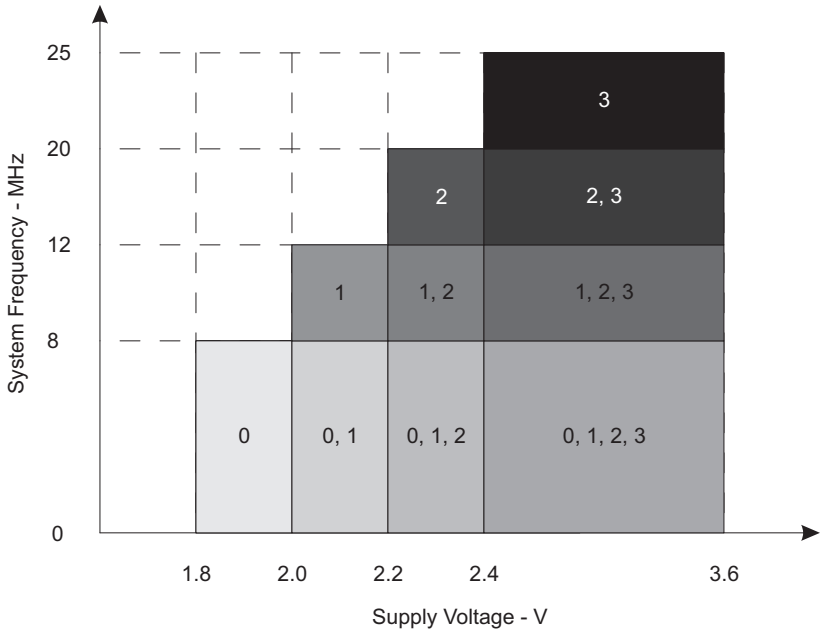

The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Frequency vs Supply Voltage

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$	Flash	3.0 V	0	0.29	0.33	1.84	2.08							mA
			1	0.32		2.08		3.10						
			2	0.33		2.24		3.50		6.37				
			3	0.35		2.36		3.70		6.75		8.90	9.60	
$I_{AM, RAM}$	RAM	3.0 V	0	0.17	0.19	0.88	0.99							mA
			1	0.18		1.00		1.47						
			2	0.19		1.13		1.68		2.82				
			3	0.20		1.20		1.78		3.00		4.50	4.90	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.

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5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		V_{CC}	PMMCOREVx	–40°C		25°C		60°C		85°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3)(4)	2.2 V	0	69	93	69	93	69	93	69	93	µA
		3.0 V	3	73	100	73	100	73	100	73	100	
I_{LPM2}	Low-power mode 2(5)(4)	2.2 V	0	11	15.5	11	15.5	11	15.5	11	15.5	µA
		3.0 V	3	11.7	17.5	11.7	17.5	11.7	17.5	11.7	17.5	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6)(4)	2.2 V	0	1.4		1.7		2.6		6.6		µA
			1	1.5		1.8		2.9		9.9		
			2	1.5		2.0		3.3		10.1		
		3.0 V	0	1.8		2.1	2.4	2.8		7.1	13.6	
			1	1.8		2.3		3.1		10.5		
			2	1.9		2.4		3.5		10.6		
			3	2.0		2.3	2.6	3.9		11.8	14.8	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(7)(4)	3.0 V	0	1.0		1.2	1.42	2.0		5.8	12.9	µA
			1	1.0		1.3		2.3		6.0		
			2	1.1		1.4		2.8		6.2		
			3	1.2		1.4	1.62	3.0		6.2	13.9	
I_{LPM4}	Low-power mode 4(8)(4)	3.0 V	0	1.1		1.2	1.35	1.9		5.7	12.9	µA
			1	1.2		1.2		2.2		5.9		
			2	1.3		1.3		2.6		6.1		
			3	1.3		1.3	1.52	2.9		6.2	13.9	
$I_{LPM4.5}$	Low-power mode 4.5(9)	3.0 V		0.10		0.10	0.13	0.20		0.50	1.14	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 1 MHz
(4) Current for brownout, high side supervisor (SVS_H) normal mode included. Low-side supervisor and monitors disabled (SVS_L, SVM_L). High-side monitor disabled (SVM_H). RAM retention enabled.
(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, $f_{SMCLK} = f_{DCO}$ = 0 MHz, DCO setting = 1 MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz
(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), $f_{ACLK} = f_{VLO}$, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ = 0 MHz
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(9) Internal regulator disabled. No data retention. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5), $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz

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5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

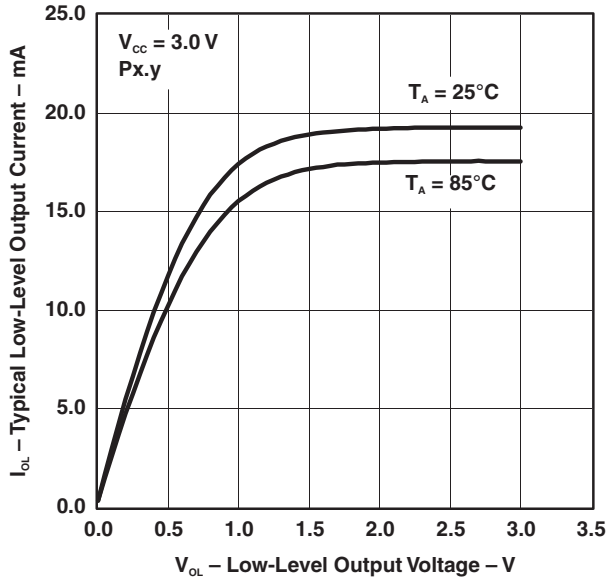

Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

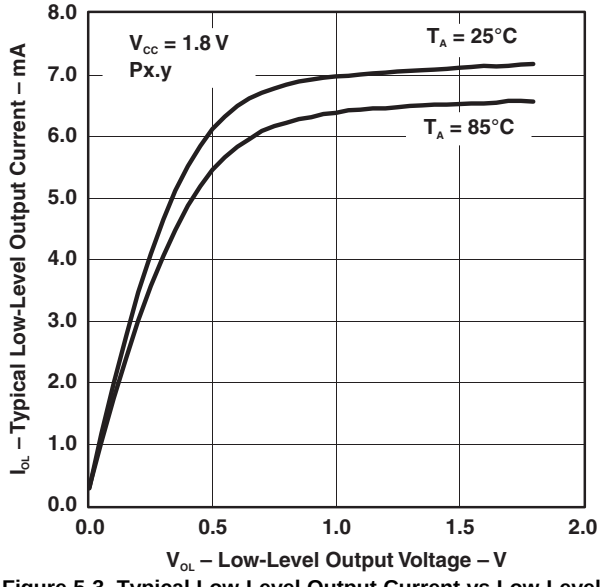

Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

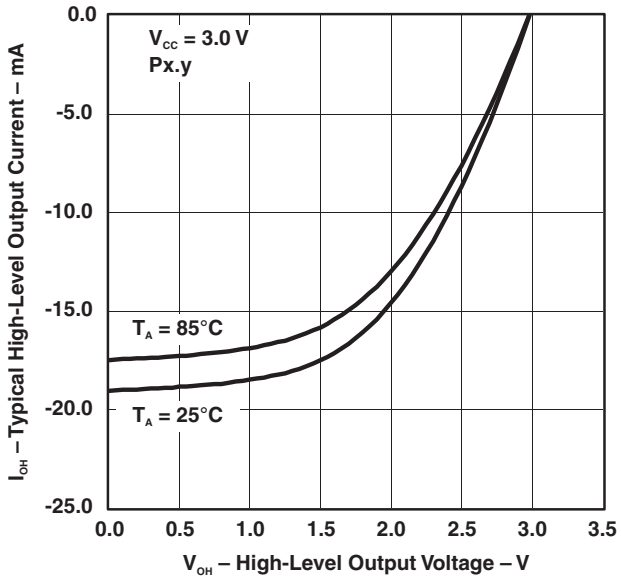

Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

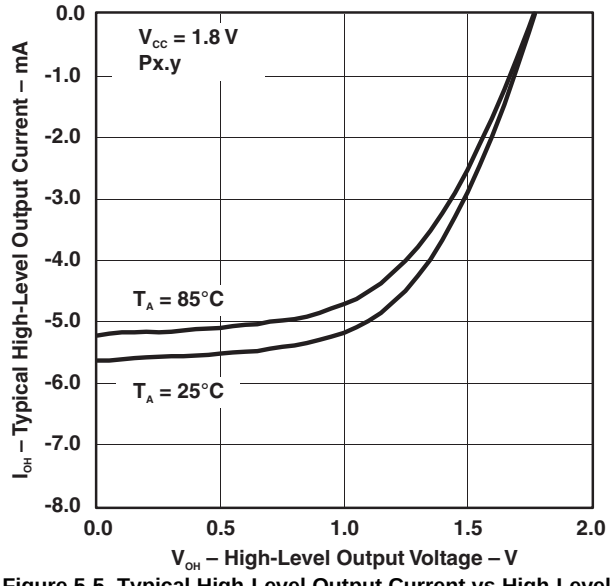

Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

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5.36 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC12 analog input pins Ax		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AVCC terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz(4)	2.2 V		125	155	µA
			3 V		150	220	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R_I	Input MUX ON-resistance	0 V ≤ V_{Ax} ≤ AVCC		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See Section 5.41 and Section 5.42.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.
(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

5.37 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC conversion clock	For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference.(1)	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference.(2)		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference.(3)		0.45	2.4	2.7	
$f_{ADC12OSC}$	Internal ADC12 oscillator(4)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			(5)		
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 1000 Ω, C_I = 20 pF, τ = [R_S + R_I] × C_I (6)	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5.0 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(5) 13 × ADC12DIV × 1/$f_{ADC12CLK}$
(6) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

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5.38 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(1)	1.4 V ≤ dVREF ≤ 1.6 V(2)	2.2 V, 3 V			±2.0	LSB
		1.6 V < dVREF(2)				±1.7	
E_D	Differential linearity error(1)	(2)	2.2 V, 3 V			±1.0	LSB
E_O	Offset error(3)	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±1.0	±2.0	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±1.0	±2.0	
E_G	Gain error(3)	(2)	2.2 V, 3 V		±1.0	±2.0	LSB
E_T	Total unadjusted error	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±1.4	±3.5	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±1.4	±3.5	

(1) Parameters are derived using the histogram method.
(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = $V_{R+} – V_{R–}$, V_{R+} < AVCC, $V_{R–}$ > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).
(3) Parameters are derived using a best fit curve.

5.39 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V			±1.7	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±2.5	
E_D	Differential linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V	–1.0		+1.5	LSB
		ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 2.7 MHz		–1.0		+1.0	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz		–1.0		+2.5	
E_O	Offset error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2.0	±4.0	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±2.0	±4.0	
E_G	Gain error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1.0	±2.5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1.5%(4)	VREF
E_T	Total unadjusted error	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2	±5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1.5%(4)	VREF

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = $V_{R+} – V_{R–}$.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

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Tema n. 2

Il candidato, dopo l'abilitazione e l'iscrizione all'Ordine degli Ingegneri, potrà svolgere la professione regolamentata di Ingegnere dell'informazione, ex articolo 46 del DPR 328/01. In tale veste supponga di ricevere l'incarico dall'ente pubblico A per redigere un progetto su come procedere per diagnosticare lo "stato di salute" del sistema informatico, parte preponderante ed essenziale del sistema informativo, operativo e decisionale dell'ente stesso.

Il Consiglio d'Amministrazione dell'ente, in base ai risultati della diagnosi di cui sopra, si propone di "curare" il sistema informatico per evitare in futuro i numerosi incidenti, subiti negli ultimi tempi, che hanno intaccato l'immagine dell'ente sul piano dell'affidabilità, dell'efficacia e dell'efficienza.
Tali incidenti si possono classificare come segue: virus e worm; accessi non autorizzati al sistema con diffusione di dati riservati; immissione di dati fake; defacing di siti web; improvvise e lunghe interruzioni dei servizi erogati online, con conseguente protesta pubblica degli utenti danneggiati.
Il sistema informatico dell'ente A è inoltre collegato, mediante interfacce automatizzate, ai sistemi informatici degli enti pubblici B, C e D, con i quali scambia giornalmente dati di ogni tipo. Questi enti sono stati anch'essi coinvolti negli incidenti per il cosiddetto "effetto domino" provocando disagi sui loro rispettivi utenti.

Le caratteristiche dell'ente A sono: ha circa 2.000 dipendenti tra stabili e precari; è suddiviso in 15 Direzioni, ciascuna costituita mediamente da 6 uffici, anche dislocati in continenti diversi; possiede un data center, una piattaforma cloud, un Autonumous System di rete, alcune decine di server e un migliaio di postazioni fisse e mobili. Il candidato, tenendo conto di tali caratteristiche, delinei ed illustri come procedere per svolgere l'incarico ricevuto.
In particolare esponga come effettuare la diagnosi sulle apparecchiature di rete, sulle componenti software, sulle procedure di sicurezza e salvaguardia della privacy, sulle procedure per l'integrità e la coerenza dei dati, per il backup e il disaster recovery, sull'istruzione e sensibilizzazione del personale dipendente circa le rilevanti responsabilità, anche penali, per la diffusione di dati riservati e sui rischi degli attacchi di social engineering.

Tema n. 3

Si supponga di dover progettare un sistema radio punto-punto capace di coprire una distanza di 1000 m, operando su una banda di ampiezza 20 MHz centrata attorno alla frequenza di 1900 MHz, fornendo una bit-rate pari ad almeno 100 Mbps

1. Si scelgano valori realistici per le seguenti grandezze e parametri:

a. Tipo di filtro di trasmissione e di ricezione
b. Tipo e guadagni di antenna in trasmissione (dispositivo mobile) ed in ricezione (base station)
c. Cifra di rumore

Come canale di trasmissione semplificato si consideri un collegamento in piena vista.

2. Si supponga un margine di 30 dB e si discuta quali sono tutte le perdite aggiuntive che questo margine deve neutralizzare.

Si supponga di dover garantire una probabilità di errore pari a 1e-6

3. Si calcoli la potenza di trasmissione necessaria per soddisfare i requisiti indicati.

Si discuta almeno uno dei due punti seguenti:

- Procedure di posizionamento meccanico e puntamento delle antenne.
- Normative da osservare in relazione all’esposizione da campi elettromagnetici in base alle normative vigenti.