**POLITECNICO DI TORINO**
**ESAMI DI STATO PER L'ABILITAZIONE ALL'ESERCIZIO**
**DELLA PROFESSIONE DI INGEGNERE DELL'INFORMAZIONE**

**II Sessione 2018 - Sezione A**
**Settore dell'Informazione**

**Prova PRATICA del 21 dicembre 2018**

*Il Candidato svolga uno a scelta fra i seguenti temi proposti.*
*Gli elaborati prodotti dovranno essere stilati in forma chiara, ordinata, sintetica e leggibile.*
*La completezza, l'attinenza e la chiarezza espositiva costituiranno elementi di valutazione.*

Tema n. 1

Il candidato progetti un sistema elettronico che riceve in ingresso un segnale audio analogico (1 Vrms, 600 Ohm) in grado di pilotare delle cuffie (100 mW, 32 Ohm).
Discuta quindi come generare le tensioni di alimentazioni necessarie.
Infine, il candidato valuti ed ottimizzi l'efficienza del circuito proposto.

Materiale:
- Datasheet OPA1688
- Datasheet TL082

TEXAS INSTRUMENTS
Burr-Brown Audio

OPA1688, OPA1689
SBOS724 – SEPTEMBER 2015

# OPA168x
# SoundPlus 36-V, Single-Supply, 10-MHz, Rail-to-Rail Output Operational Amplifiers

## 1 Features

- THD+N, 50 mW, 32 Ω, 1 kHz, –109 dB
- Wide Supply Range:
  - 4.5 V to 36 V, ±2.25 V to ±18 V
- Low Offset Voltage: ±0.25 mV
- Low Offset Drift: ±0.5 µV/°C
- Gain Bandwidth: 10 MHz
- Low Input Bias Current: ±10 pA
- Low Quiescent Current: 1.6 mA per Amplifier
- Low Noise: 8 nV/√Hz
- EMI- and RFI-Filtered Inputs
- Input Range Includes Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- High Common-Mode Rejection: 120 dB
- Industry-Standard Packages:
  - SOIC-8 and SOIC-14
- *micro*Packages:
  - Dual in WSON-8, Quad in VQFN-16

## 2 Applications

- Headphone Driver
- Analog and Digital Mixers
- Audio Effects Processors
- Transducer Amplifiers
- Musical Instruments
- A/V Receivers
- DVD and Blu-Ray™ Players
- Car Audio Systems

## 3 Description

The OPA1688 and OPA1689 are a family of SoundPlus™ 36-V, single-supply, low-noise operational amplifiers capable of operating on supplies ranging from 4.5 V (±2.25 V) to 36 V (±18 V). This latest addition of high-voltage audio operational amplifiers, in conjunction with the OPA16xx devices provide a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications. The OPA168x are available in micropackages, and offer low offset, drift, and quiescent current. These devices also offer wide bandwidth, fast slew rate, and high output current drive capability. The dual and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps that are specified at only one supply voltage, the OPA168x family is specified from 4.5 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The OPA168x series of op amps are specified from –40°C to 85°C.

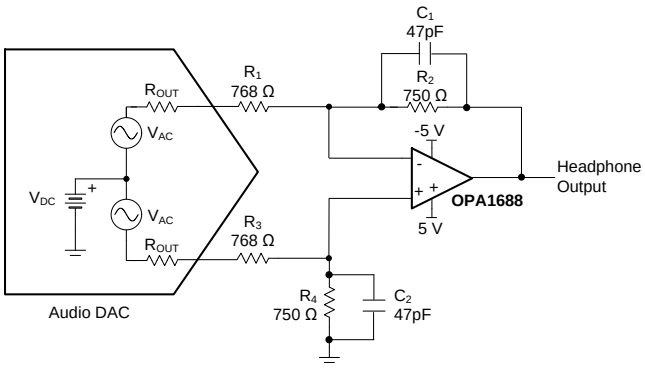
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| OPA1688 | SOIC (8) | 4.90 mm × 3.91 mm |
| | WSON (8) | 3.00 mm × 3.00 mm |
| OPA1689(2) | SOIC (14) | 8.65 mm × 3.91 mm |
| | VQFN (16) | 3.50 mm × 3.50 mm |

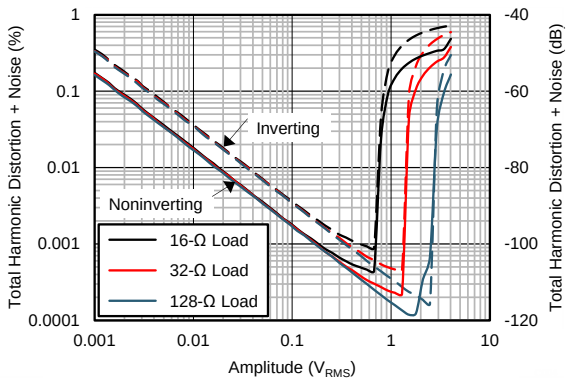
(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Product-preview device.

**Headphone Amplifier Circuit Configuration**




**Superior THD Performance (f = 1 kHz, BW = 80 kHz, $V_S$ = ±5 V)**



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## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| September 2015 | * | Initial release. |

## 5 Device Comparison Table

| DEVICE(1) | PACKAGE |
|---|---|
| OPA1688 (dual) | SOIC-8, WSON-8 |
| OPA1689 (quad) | SOIC-14, VQFN-16 |

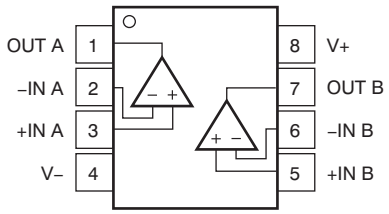
(1) The OPA1688 SOIC-8 and WSON-8 packages are production data. The OPA1689 SOIC-14 and VQFN-16 packages are product preview.

## 6 Device Family Comparison Table

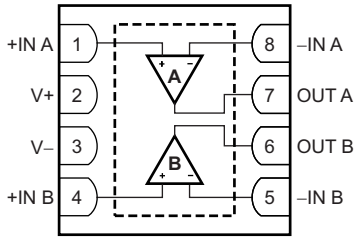
| DEVICE | QUIESCENT CURRENT ($I_Q$) | GAIN BANDWIDTH PRODUCT (GBP) | VOLTAGE NOISE DENSITY ($e_n$) |
|---|---|---|---|
| OPA168x | 1650 µA | 10 MHz | 8 nV/√Hz |
| OPA165x | 2000 µA | 18 MHz | 4.5 nV/√Hz |
| OPA166x | 1500 µA | 22 MHz | 3.3 nV/√Hz |

## 7 Pin Configuration and Functions

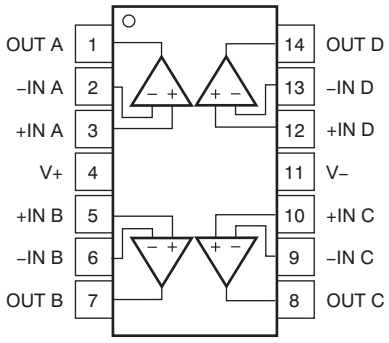
**D Package: OPA1688**
**SOIC-8**
**Top View**



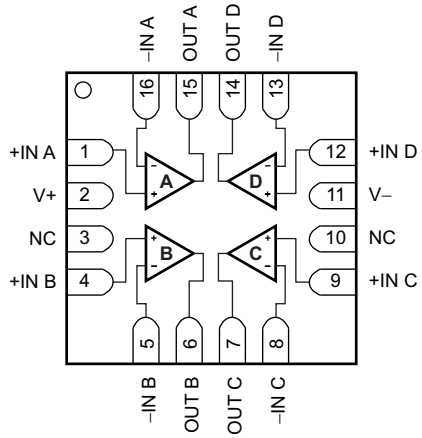

**DRG Package: OPA1688**
**WSON-8**
**Top View**




**D Package: OPA1689**
**SOIC-14**
**Top View**




**RVA Package: OPA1689**
**VQFN-16**
**Top View**



### Pin Functions: OPA1688

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| | OPA1688 | | | |
| NAME | D (SOIC) | DRG (WSON) | | |
| +IN A | 3 | 1 | I | Noninverting input, channel A |
| +IN B | 5 | 4 | I | Noninverting input, channel B |
| –IN A | 2 | 8 | I | Inverting input, channel A |
| –IN B | 6 | 5 | I | Inverting input, channel B |
| OUT A | 1 | 7 | O | Output, channel A |
| OUT B | 7 | 6 | O | Output, channel B |
| V+ | 8 | 2 | — | Positive (highest) power supply |
| V– | 4 | 3 | — | Negative (lowest) power supply |

### Pin Functions: OPA1689

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| | OPA1689 | | | |
| NAME | D | RVA | | |
| +IN A | 3 | 1 | I | Noninverting input, channel A |
| +IN B | 5 | 4 | I | Noninverting input, channel B |
| +IN C | 10 | 9 | I | Noninverting input, channel C |
| +IN D | 12 | 12 | I | Noninverting input, channel D |
| –IN A | 2 | 16 | I | Inverting input, channel A |
| –IN B | 6 | 5 | I | Inverting input, channel B |
| –IN C | 9 | 8 | I | Inverting input, channel C |
| –IN D | 13 | 13 | I | Inverting input, channel D |
| OUT A | 1 | 15 | O | Output, channel A |
| OUT B | 7 | 6 | O | Output, channel B |
| OUT C | 8 | 7 | O | Output, channel C |
| OUT D | 14 | 14 | O | Output, channel D |
| V+ | 4 | 2 | — | Positive (highest) power supply |
| V– | 11 | 11 | — | Negative (lowest) power supply |
| NC | — | 3, 10 | — | No connection |

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_S$ | | | | ±20 (40, single supply) | V |
| Signal input pins | Voltage(2) | Common-mode | (V–) – 0.5 | (V+) + 0.5 | V |
| | | Differential(3) | | ±0.5 | V |
| | Current | | | ±10 | mA |
| Output short circuit(4) | | | | Continuous | |
| Temperature | Temperature range | | –55 | 150 | °C |
| | Junction temperature | | | 150 | °C |
| | Storage, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings should be current limited to 10 mA or less.
(3) See the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage (V+ – V–) | 4.5 (±2.25) | | 36 (±18) | V |
| Specified temperature | –40 | | 85 | °C |

## 8.4 Thermal Information: OPA1688

| THERMAL METRIC(1) | | OPA1688 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DRG (WSON) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 116.1 | 63.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 69.8 | 63.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.6 | 36.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 22.5 | 1.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.1 | 36.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 6.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 8.5 Thermal Information: OPA1689

| THERMAL METRIC(1) | | OPA1689 | | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | RVA (VQFN) | |
| | | 14 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 82.7 | TBD | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42.3 | TBD | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 37.3 | TBD | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 8.9 | TBD | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 37 | TBD | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | TBD | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 8.6 Electrical Characteristics

At $T_A$ = 25°C, $V_S$ = ±2.25 V to ±18 V, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **AUDIO PERFORMANCE** | | | | | | |
| THD+N | Total harmonic distortion + noise | G = 1, f = 1 kHz, $V_O$ = 3.5 $V_{RMS}$ , $R_L$ = 2 kΩ | | 0.00005% | | |
| | | | | –126 | | dB |
| | | G = 1, f = 1 kHz, $V_O$ = 3.5 $V_{RMS}$ , $R_L$ = 600 Ω | | 0.000051% | | |
| | | | | –126 | | dB |
| | | G = 1, f = 1 kHz, $P_O$ = 10 mW, $R_L$ = 128 Ω | | 0.000153% | | |
| | | | | –116 | | dB |
| | | G = 1, f = 1 kHz, $P_O$ = 10 mW, $R_L$ = 32 Ω | | 0.000357% | | |
| | | | | –109 | | dB |
| | | G = 1, f = 1 kHz, $P_O$ = 10 mW, $R_L$ = 16 Ω | | 0.000616% | | |
| | | | | –104 | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| GBP | Gain bandwidth product | G = 1 | | 10 | | MHz |
| SR | Slew rate | G = 1 | | 8 | | V/µs |
| | Full-power bandwidth(1) | $V_O$ = 1 $V_{PP}$ | | 1.3 | | MHz |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | 200 | | ns |
| | Channel separation (dual) | f = 1 kHz | | –120 | | dB |
| $t_S$ | Settling time | To 0.1%, $V_S$ = ±18 V, G = 1, 10-V step | | 3 | | µs |
| **NOISE** | | | | | | |
| $E_n$ | Input voltage noise | f = 0.1 Hz to 10 Hz | | 2.5 | | $\mu V_{PP}$ |
| $e_n$ | Input voltage noise density(2) | f = 100 Hz | | 14 | | $nV/\sqrt{Hz}$ |
| | | f = 1 kHz | | 8 | | |
| $i_n$ | Input current noise density | f = 1 kHz | | 1.8 | | $fA/\sqrt{Hz}$ |
| **OFFSET VOLTAGE** | | | | | | |
| $V_{OS}$ | Input offset voltage | $T_A$ = 25°C | | ±0.25 | ±1.5 | mV |
| | | $T_A$ = –40°C to 85°C | | | ±1.6 | |
| $dV_{OS}/dT$ | $V_{OS}$ over temperature(2) | $T_A$ = –40°C to 85°C | | ±0.5 | ±2 | µV/°C |
| PSRR | Power-supply rejection ratio | $T_A$ = –40°C to 85°C | | ±1 | ±2.5 | µV/V |
| | Channel separation, dc | At dc | | 0.1 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| $I_B$ | Input bias current | $T_A$ = 25°C | | ±10 | ±20 | pA |
| | | $T_A$ = –40°C to 85°C | | | ±1.5 | nA |
| $I_{OS}$ | Input offset current | $T_A$ = 25°C | | ±3 | ±7 | pA |
| | | $T_A$ = –40°C to 85°C | | | ±250 | pA |
| **INPUT VOLTAGE RANGE** | | | | | | |
| $V_{CM}$ | Common-mode voltage range(3) | | (V–) – 0.1 V | | (V+) – 2 V | V |
| CMRR | Common-mode rejection ratio | $V_S$ = ±2.25 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V, $T_A$ = –40°C to 85°C | 90 | 104 | | dB |
| | | $V_S$ = ±18 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V, $T_A$ = –40°C to 85°C | 104 | 120 | | |
| **INPUT IMPEDANCE** | | | | | | |
| | Differential | | | 100 \|\| 7 | | MΩ \|\| pF |
| | Common-mode | | | 6 \|\| 1.5 | | $10^{12}$Ω \|\| pF |

(1) Full-power bandwidth = SR / (2π × $V_P$), where SR = slew rate.
(2) Specified by design and characterization.
(3) Common-mode range can extend to the top rail with reduced performance.

## Electrical Characteristics (continued)

At $T_A$ = 25°C, $V_S$ = ±2.25 V to ±18 V, $V_{CM}$ = $V_{OUT}$ = $V_S$ / 2, and $R_L$ = 10 kΩ connected to $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OPEN-LOOP GAIN** | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | (V–) + 0.35 V < $V_O$ < (V+) – 0.35 V, $R_L$ = 10 kΩ, $T_A$ = –40°C to 85°C | 108 | 130 | | dB |
| | | (V–) + 0.5 V < $V_O$ < (V+) – 0.5 V, $R_L$ = 2 kΩ, $T_A$ = –40°C to 85°C | | 118 | | |
| **OUTPUT** | | | | | | |
| $V_O$ | Voltage output swing from rail | $I_L$ = ±1 mA | (V–) + 0.1 V | | (V+) – 0.1 V | mV |
| | | $V_S$ = 36 V, $R_L$ = 10 kΩ | | 70 | 90 | |
| | | $V_S$ = 36 V, $R_L$ = 2 kΩ | | 330 | 400 | |
| $Z_O$ | Open-loop output impedance | f = 1 MHz, $I_O$ = 0 A | | 60 | | Ω |
| $I_{SC}$ | Short-circuit current | | | ±75 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | See the *Typical Characteristics* | | | pF |
| **POWER SUPPLY** | | | | | | |
| $V_S$ | Specified voltage range | | 4.5 | | 36 | V |
| $I_Q$ | Quiescent current per amplifier | $I_O$ = 0 A | | 1.6 | 1.8 | mA |
| | | $I_O$ = 0 A, $T_A$ = –40°C to 85°C | | | 2 | |
| **TEMPERATURE RANGE** | | | | | | |
| | Specified range | | –40 | | 85 | °C |
| | Operating range | | –55 | | 125 | °C |

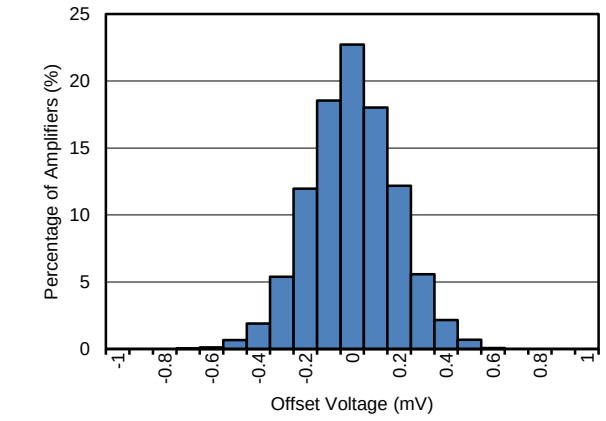
## 8.7 Typical Characteristics: Table of Graphs

**Table 1. List of Typical Characteristics**

| DESCRIPTION | FIGURE |
|---|---|
| Offset Voltage Production Distribution | Figure 1 |
| Offset Voltage Drift Distribution | Figure 2 |
| Offset Voltage vs Temperature ($V_S$ = ±18 V) | Figure 3 |
| Offset Voltage vs Common-Mode Voltage ($V_S$ = ±18 V) | Figure 4 |
| Offset Voltage vs Common-Mode Voltage (Upper Stage) | Figure 5 |
| Offset Voltage vs Power Supply | Figure 6 |
| Input Bias Current vs Common-Mode Voltage | Figure 7 |
| Input Bias Current vs Temperature | Figure 8 |
| Output Voltage Swing vs Output Current (Maximum Supply) | Figure 9 |
| CMRR and PSRR vs Frequency (Referred-to-Input) | Figure 10 |
| CMRR vs Temperature | Figure 11 |
| PSRR vs Temperature | Figure 12 |
| 0.1-Hz to 10-Hz Noise | Figure 13 |
| Input Voltage Noise Spectral Density vs Frequency | Figure 14 |
| THD+N Ratio vs Frequency | Figure 15 |
| THD+N vs Output Amplitude | Figure 16 |
| THD+N vs Frequency | Figure 17 |
| THD+N vs Amplitude | Figure 18 |
| Quiescent Current vs Temperature | Figure 19 |
| Quiescent Current vs Supply Voltage | Figure 20 |
| Open-Loop Gain and Phase vs Frequency | Figure 21 |
| Closed-Loop Gain vs Frequency | Figure 22 |
| Open-Loop Gain vs Temperature | Figure 23 |
| Open-Loop Output Impedance vs Frequency | Figure 24 |
| Small-Signal Overshoot vs Capacitive Load (100-mV Output Step) | Figure 25, Figure 26 |
| Positive Overload Recovery | Figure 27, Figure 28 |
| Negative Overload Recovery | Figure 29, Figure 30 |
| Small-Signal Step Response (10 mV, G = –1) | Figure 31 |
| Small-Signal Step Response (10 mV, G = 1) | Figure 32 |
| Small-Signal Step Response (100 mV, G = –1) | Figure 33 |
| Small-Signal Step Response (100 mV, G = 1) | Figure 34 |
| Large-Signal Step Response (10 V, G = –1) | Figure 35 |
| Large-Signal Step Response (10 V, G = 1) | Figure 36 |
| Large-Signal Settling Time (10-V Positive Step) | Figure 37 |
| Large-Signal Settling Time (10-V Negative Step) | Figure 38 |
| No Phase Reversal | Figure 39 |
| Short-Circuit Current vs Temperature | Figure 40 |
| Maximum Output Voltage vs Frequency | Figure 41 |
| EMIRR vs Frequency | Figure 42 |
| Channel Separation vs Frequency | Figure 43 |

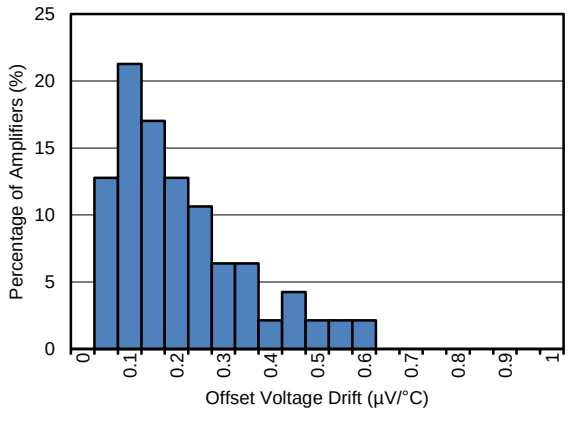
## 8.8 Typical Characteristics

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.



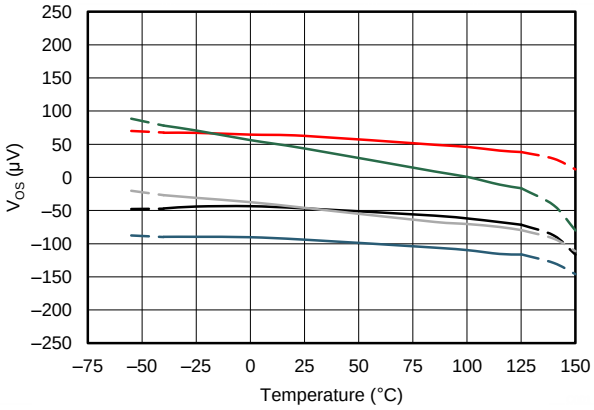

Distribution taken from 5185 amplifiers

**Figure 1. Offset Voltage Production Distribution**



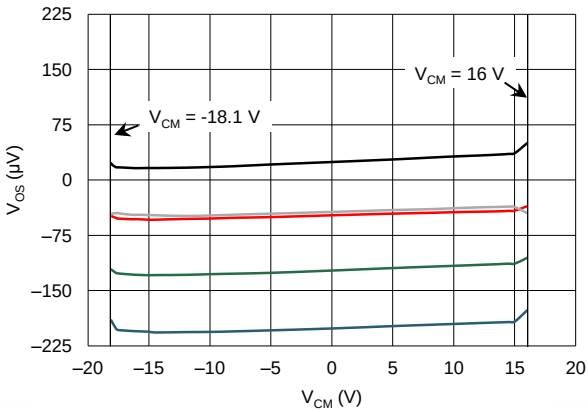

Distribution taken from 47 amplifiers,
temperature = –40°C to 125°C

**Figure 2. Offset Voltage Drift Production Distribution**



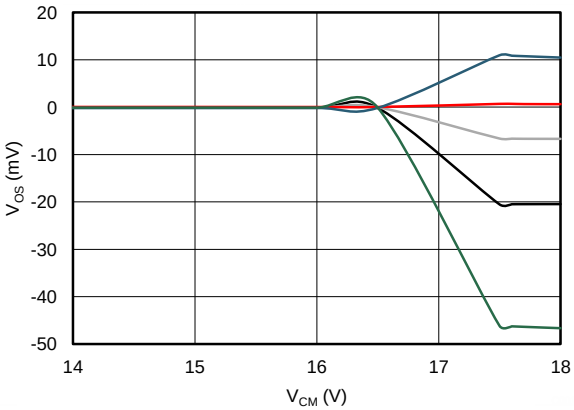

5 typical units shown, $V_S$ = ±18 V

**Figure 3. Offset Voltage vs Temperature ($V_S$ = ±18 V)**



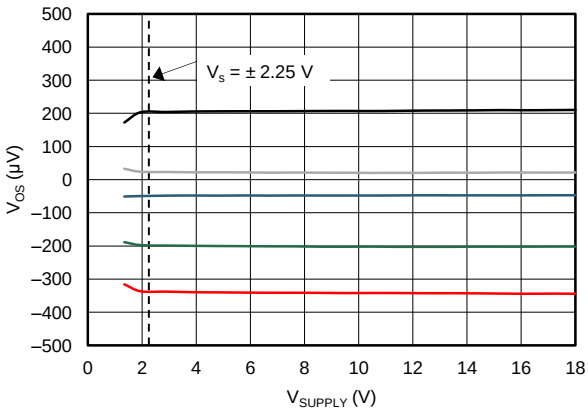

5 typical units shown, $V_S$ = ±18 V

**Figure 4. Offset Voltage vs Common-Mode Voltage ($V_S$ = ±18 V)**




5 typical units shown, $V_S$ = ±18 V

**Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)**




5 typical units shown, $V_S$ = ±2.25 V to ±18 V

**Figure 6. Offset Voltage vs Power Supply**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

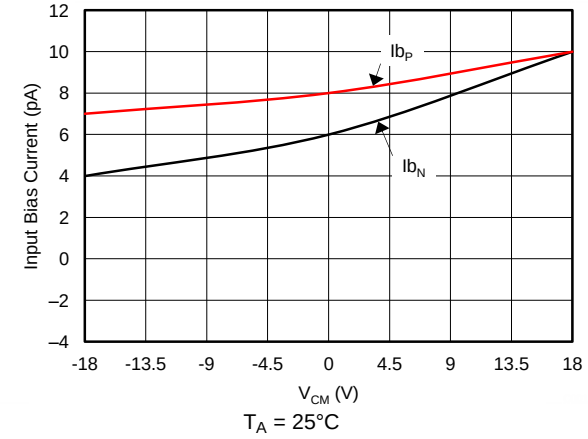



**Figure 7. Input Bias Current vs Common-Mode Voltage**

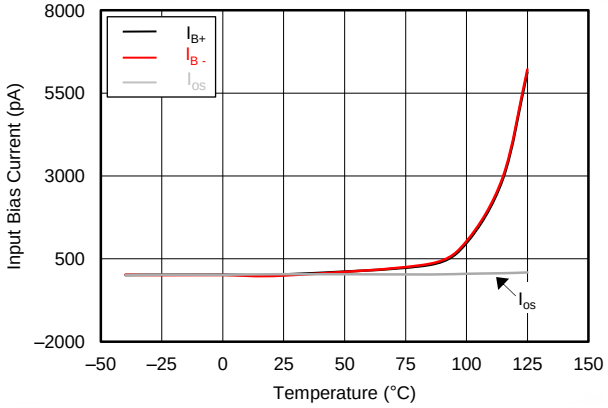



**Figure 8. Input Bias Current vs Temperature**

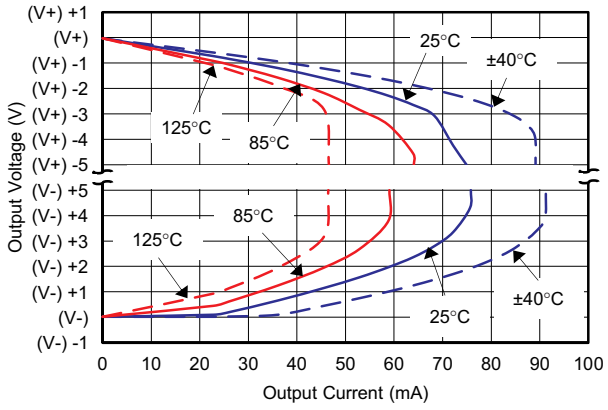



**Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)**

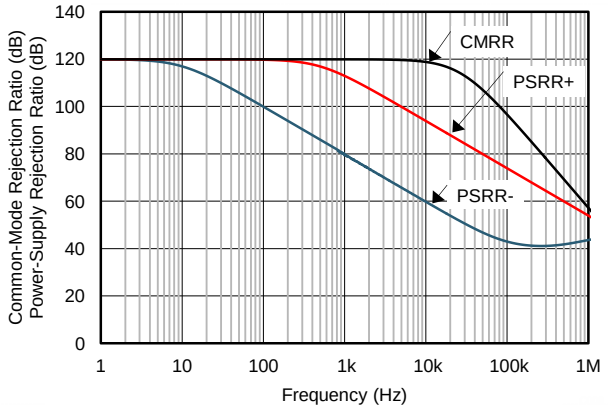



**Figure 10. CMRR and PSRR vs Frequency (Referred-to-Input)**

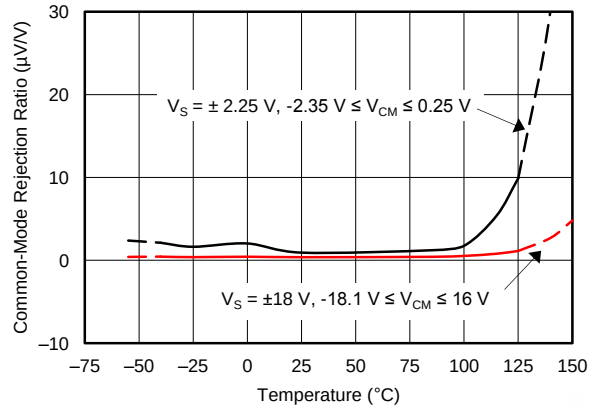



**Figure 11. CMRR vs Temperature**

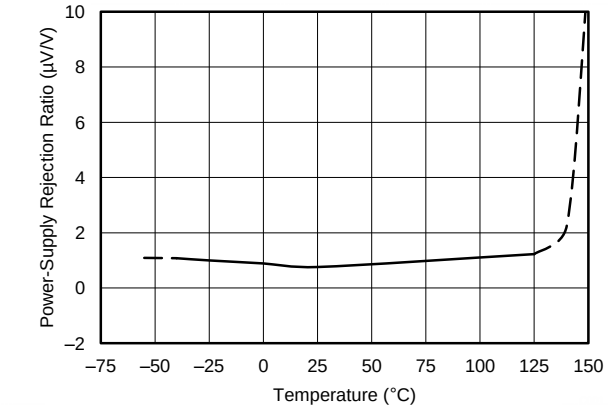
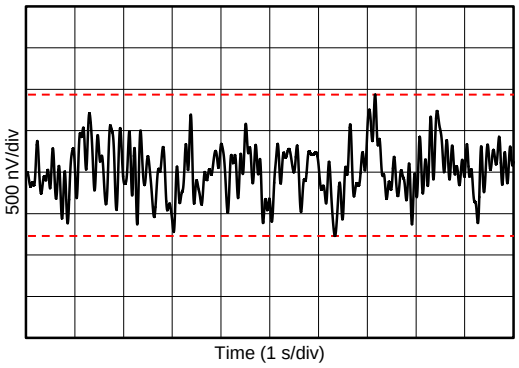



**Figure 12. PSRR vs Temperature**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.




Peak-to-peak noise = 1.70 $\mu V_{PP}$

**Figure 13. 0.1-Hz to 10-Hz Noise**

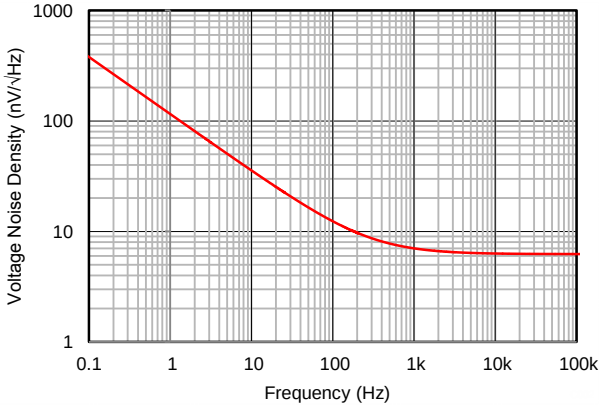
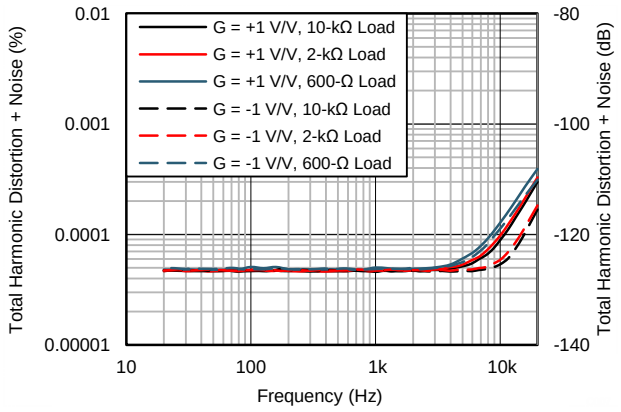
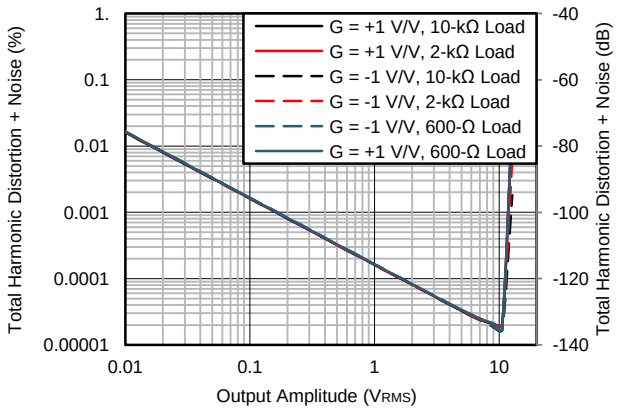



**Figure 14. Input Voltage Noise Spectral Density vs Frequency**



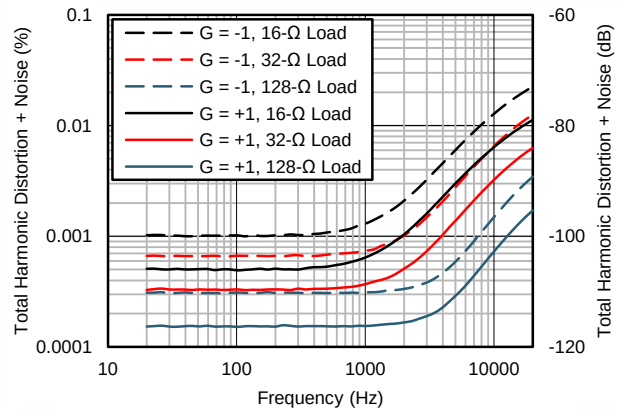

$V_{OUT}$ = 3.5 $V_{RMS}$, BW = 50 kHz

**Figure 15. THD+N Ratio vs Frequency**



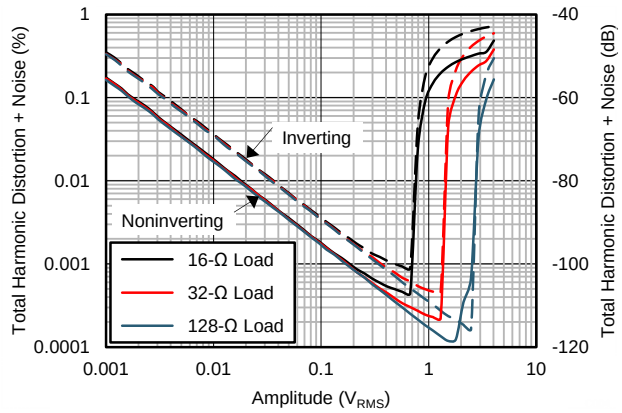

f = 1 kHz, BW = 80 kHz

**Figure 16. THD+N vs Output Amplitude**




$P_{OUT}$ = 10 mW, BW = 80 kHz, $V_S$ = ±5 V

**Figure 17. THD+N vs Frequency**




f = 1 kHz, BW = 80 kHz, $V_S$ = ±5 V

**Figure 18. THD+N vs Amplitude**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

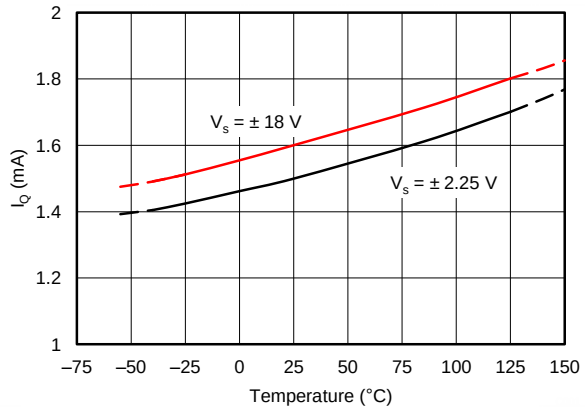



**Figure 19. Quiescent Current vs Temperature**

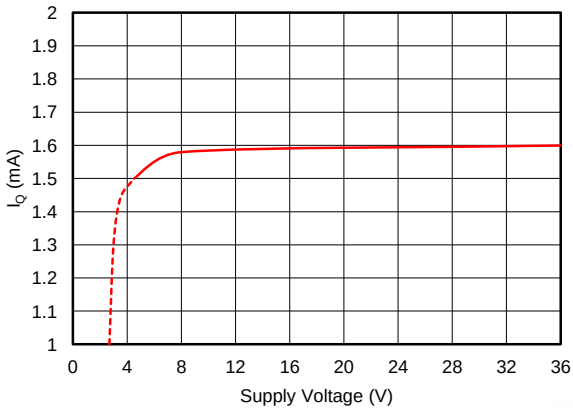
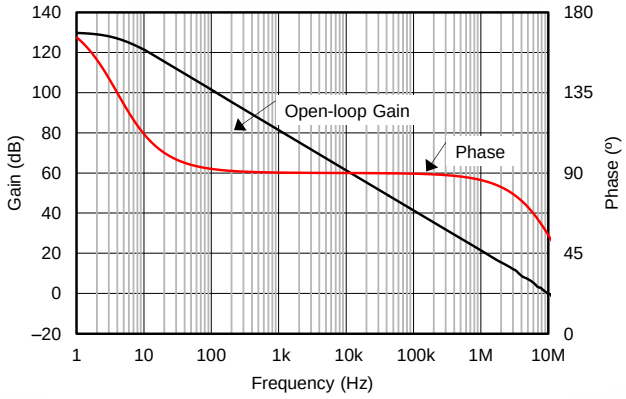



**Figure 20. Quiescent Current vs Supply Voltage**




$C_{LOAD}$ = 15 pF

**Figure 21. Open-Loop Gain and Phase vs Frequency**

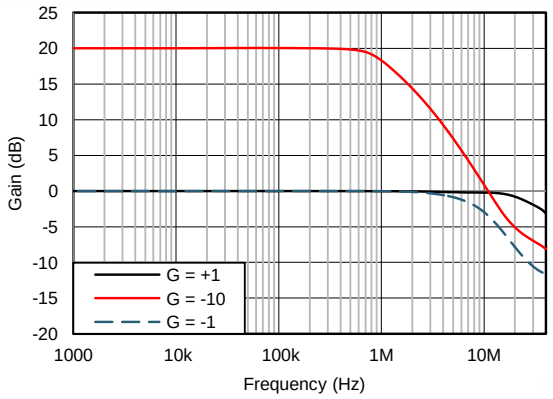
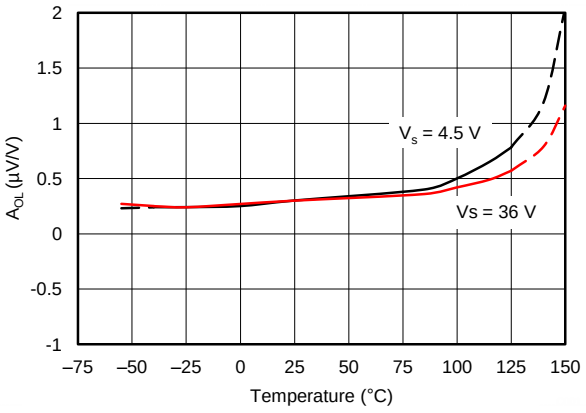



**Figure 22. Closed-Loop Gain vs Frequency**




$R_L$ = 10 kΩ

**Figure 23. Open-Loop Gain vs Temperature**

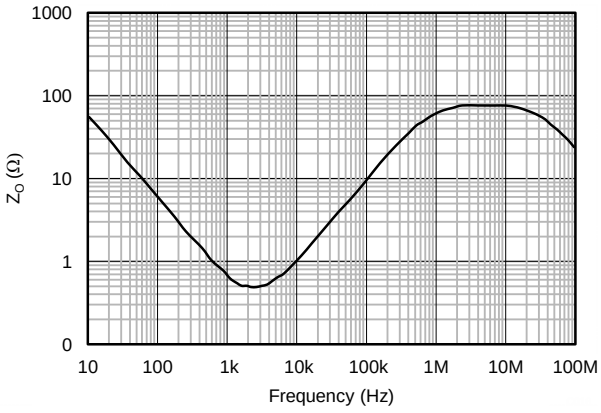



**Figure 24. Open-Loop Output Impedance vs Frequency**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

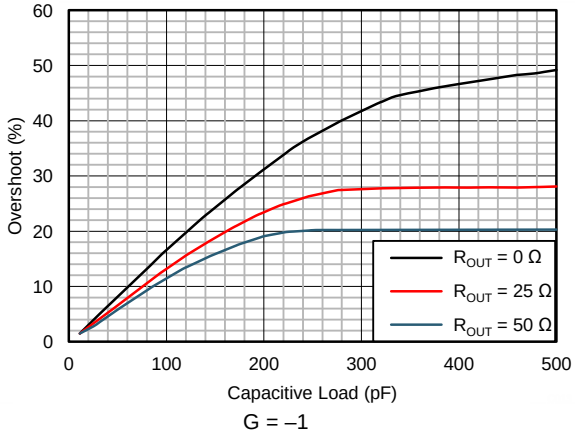



**Figure 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

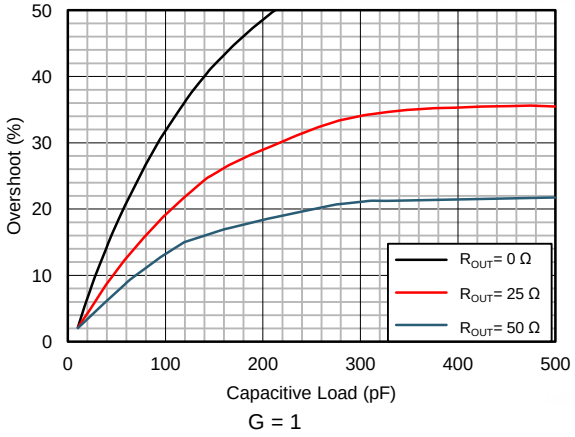



**Figure 26. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

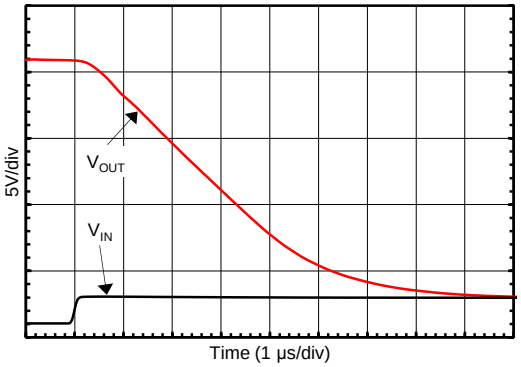



**Figure 27. Positive Overload Recovery**

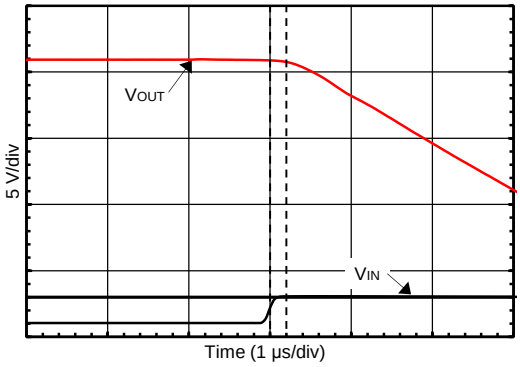



**Figure 28. Positive Overload Recovery (Zoomed In)**

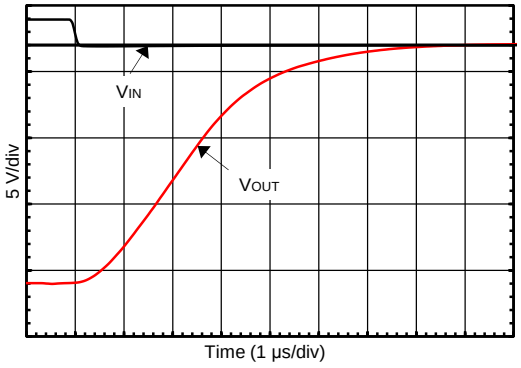



**Figure 29. Negative Overload Recovery**

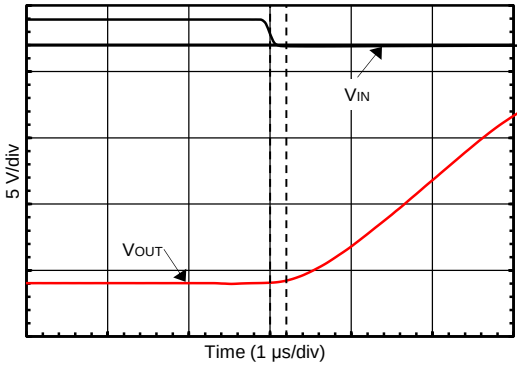
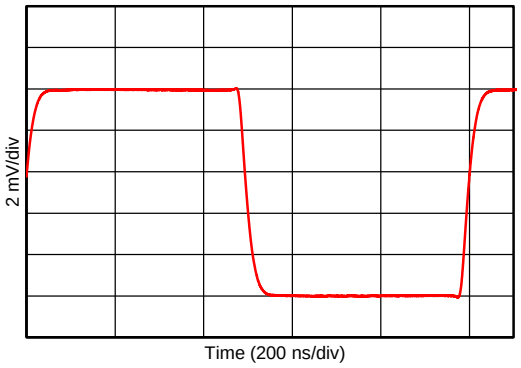



**Figure 30. Negative Overload Recovery (Zoomed In)**

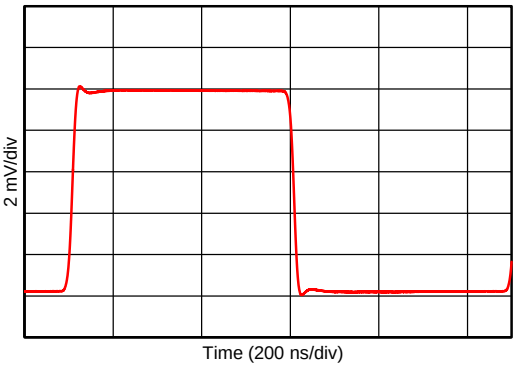
## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.



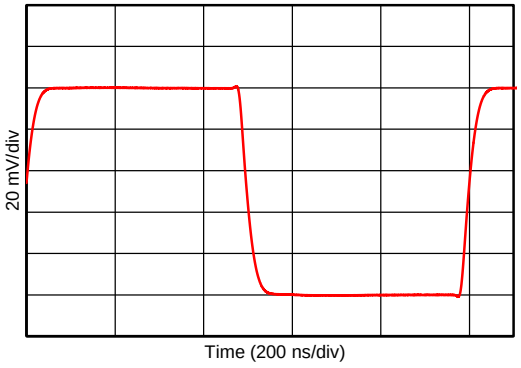

$R_L$ = 1 kΩ, $C_L$ = 10 pF

**Figure 31. Small-Signal Step Response (10 mV, G = –1)**



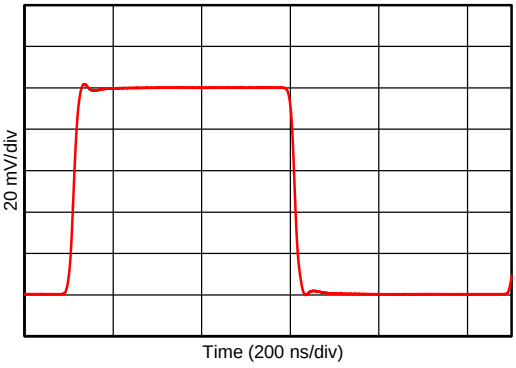

$C_L$ = 10 pF

**Figure 32. Small-Signal Step Response (10 mV, G = 1)**



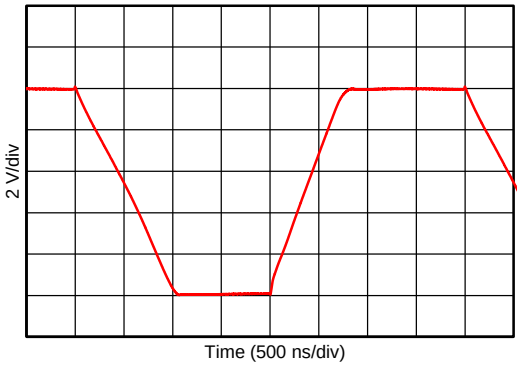

$R_L$ = 1 kΩ, $C_L$ = 10 pF

**Figure 33. Small-Signal Step Response (100 mV, G = –1)**



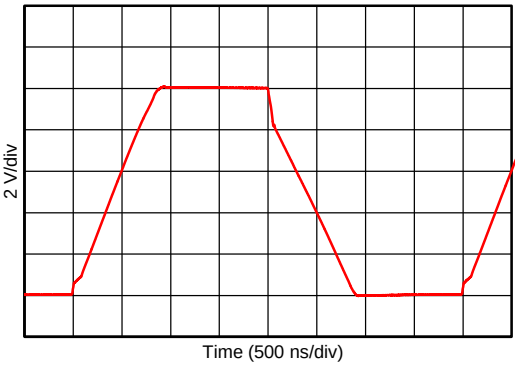

$C_L$ = 10 pF

**Figure 34. Small-Signal Step Response (100 mV, G = 1)**




$R_L$ = 1 kΩ, $C_L$ = 10 pF

**Figure 35. Large-Signal Step Response (10 V, G = –1)**

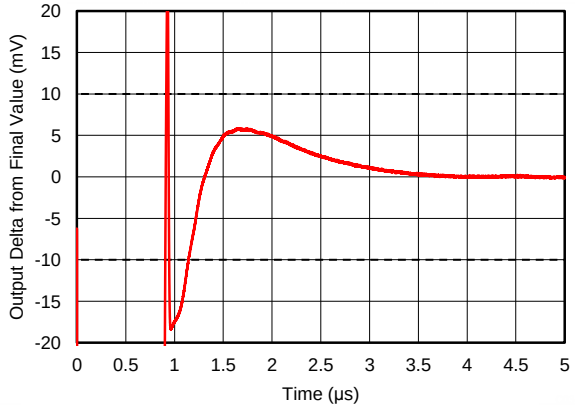



$C_L$ = 10 pF

**Figure 36. Large-Signal Step Response (10 V, G = 1)**

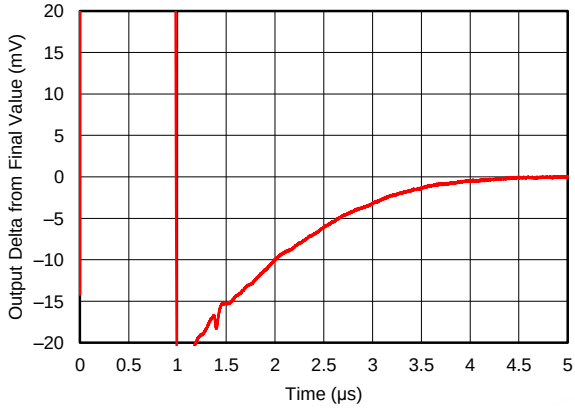
## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.




G = 1, $C_L$ = 10 pF, 0.1% settling = ±10 mV

**Figure 37. Large-Signal Settling Time (10-V Positive Step)**




G = 1, $C_L$ = 10 pF, 0.1% settling = ±10 mV

**Figure 38. Large-Signal Settling Time (10-V Negative Step)**

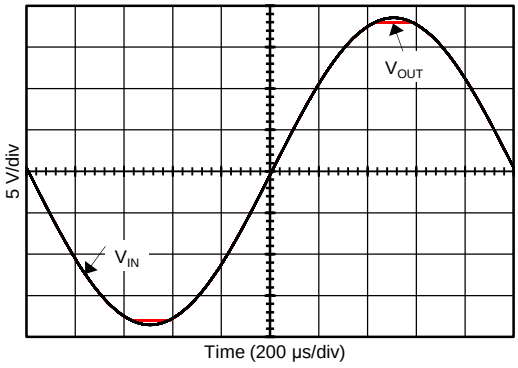



**Figure 39. No Phase Reversal**

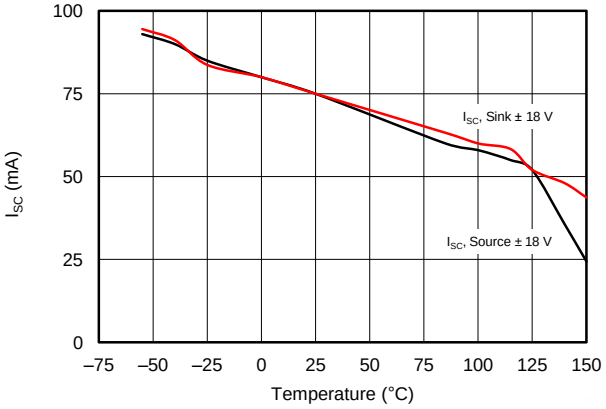



**Figure 40. Short-Circuit Current vs Temperature**

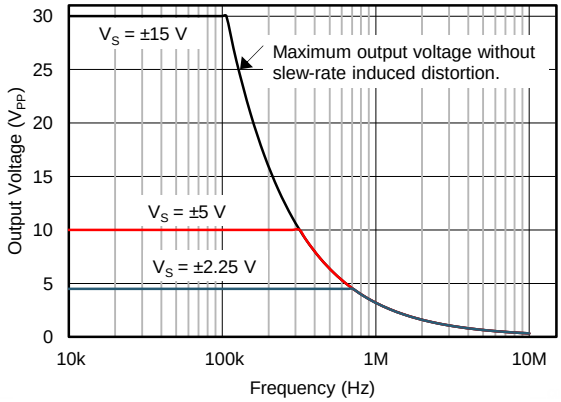
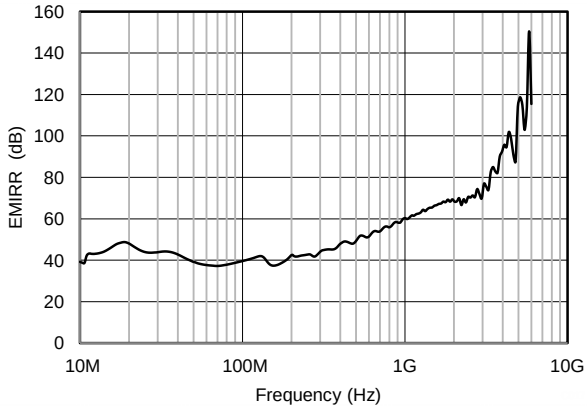



**Figure 41. Maximum Output Voltage vs Frequency**




$P_{RF}$ = –10 dBm, $V_{SUPPLY}$ = ±18 V, $V_{CM}$ = 0 V

**Figure 42. EMIRR vs Frequency**

## Typical Characteristics (continued)

$V_S$ = ±18 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 100 pF, unless otherwise noted.

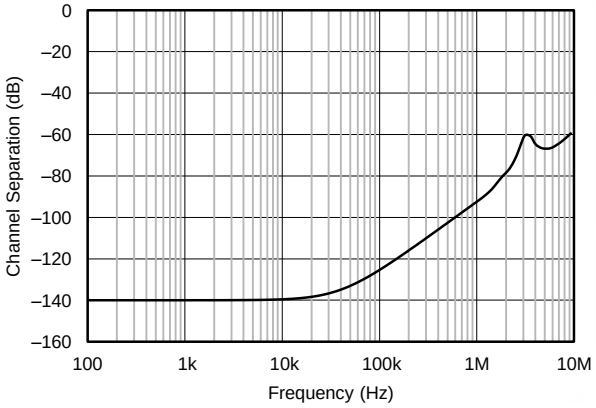



**Figure 43. Channel Separation vs Frequency**

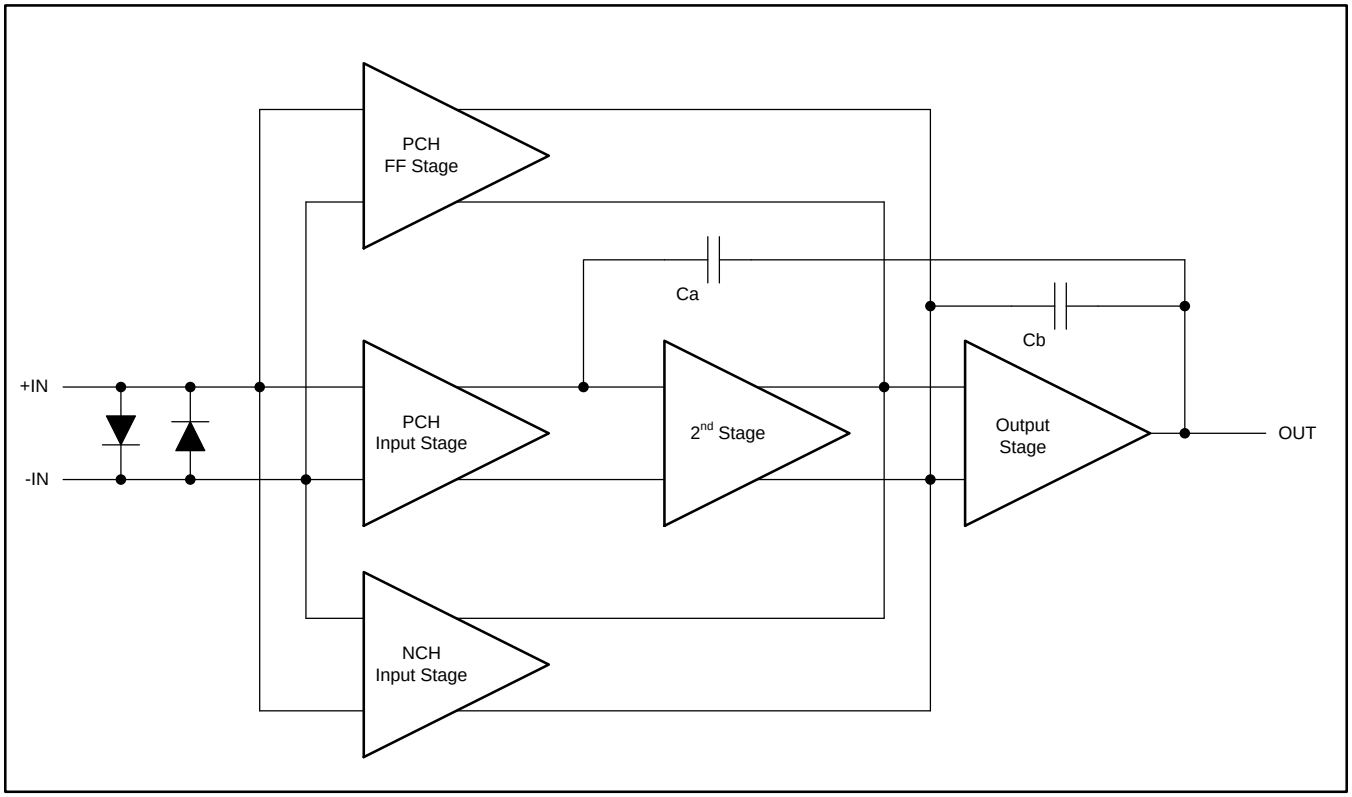
# 9 Detailed Description

## 9.1 Overview

The OPA168x family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (max) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, $A_{OL}$, and superior THD.

The *Functional Block Diagram* section shows the simplified diagram of the OPA168x design. The design topology is a highly-optimized, three-stage amplifier with an active-feedforward gain stage.

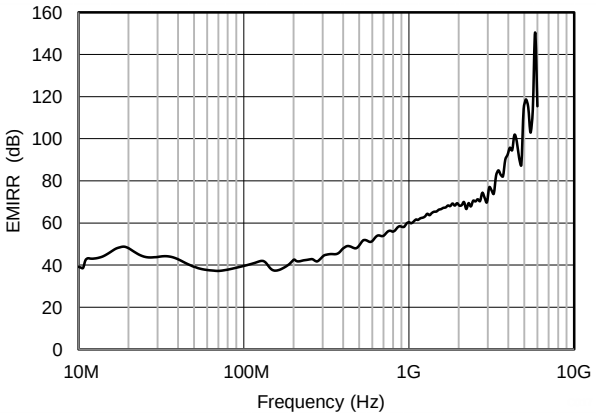
## 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 EMI Rejection

The OPA168x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA168x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 44 shows the results of this testing on the OPA168x. Table 2 shows the EMIRR IN+ values for the OPA168x at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 can be centered on or operated near the particular frequency shown. Detailed information can also be found in application report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.




$P_{RF}$ = –10 dBm, $V_{SUPPLY}$ = ±18 V, $V_{CM}$ = 0 V

**Figure 44. EMIRR Testing**

**Table 2. OPAx168x EMIRR IN+ for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|---|---|---|
| 400 MHz | Mobile radio, mobile satellite, space operation, weather, radar, and ultrahigh frequency (UHF) applications | 47.6 dB |
| 900 MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, and UHF applications | 58.5 dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, and L-band (1 GHz to 2 GHz) | 68 dB |
| 2.4 GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, and S-band (2 GHz to 4 GHz) | 69.2 dB |
| 3.6 GHz | Radiolocation, aero communication and navigation, satellite, mobile, and S-band | 82.9 dB |
| 5.0 GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, and C-band (4 GHz to 8 GHz) | 114 dB |

### 9.3.2 Phase-Reversal Protection

The OPA168x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA168x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in Figure 45.

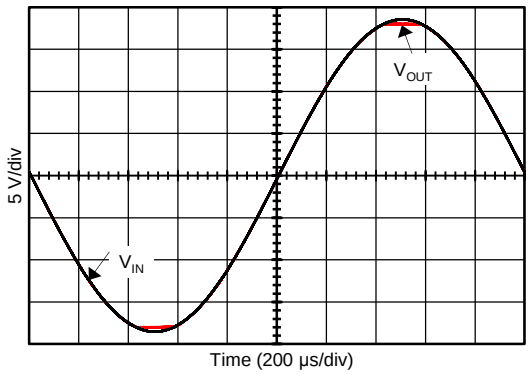



**Figure 45. No Phase Reversal**

### 9.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPA168x are optimized for commonly-used operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and may lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, $R_{OUT}$ = 50 Ω) in series with the output. Figure 46 and Figure 47 show graphs of small-signal overshoot versus capacitive load for several values of $R_{OUT}$; see application bulletin SBOA015 (AB-028), *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com, for details of analysis techniques and application circuits.

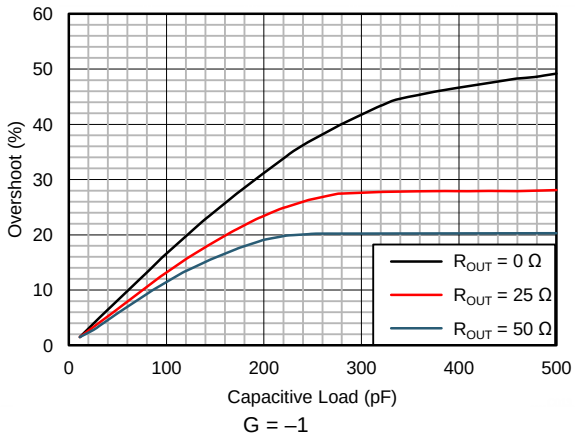



**Figure 46. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

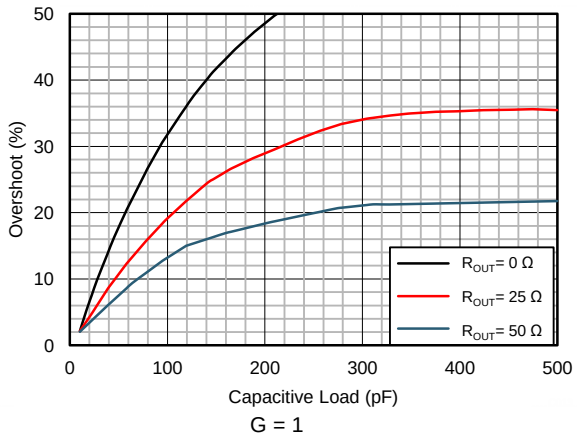



**Figure 47. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)**

## 9.4 Device Functional Modes

### 9.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPA168x series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 3.

**Table 3. Typical Performance Range ($V_S$ = ±18 V)**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Input common-mode voltage | (V+) – 2 | | (V+) + 0.1 | V |
| Offset voltage | | 5 | | mV |
| Offset voltage vs temperature ($T_A$ = –40°C to 85°C) | | 10 | | µV/°C |
| Common-mode rejection | | 70 | | dB |
| Open-loop gain | | 60 | | dB |
| Gain bandwidth product (GBP) | | 4 | | MHz |
| Slew rate | | 4 | | V/µs |
| Noise at f = 1 kHz | | 22 | | nV/√Hz |

### 9.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 48 illustrates the ESD circuits contained in the OPA168x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

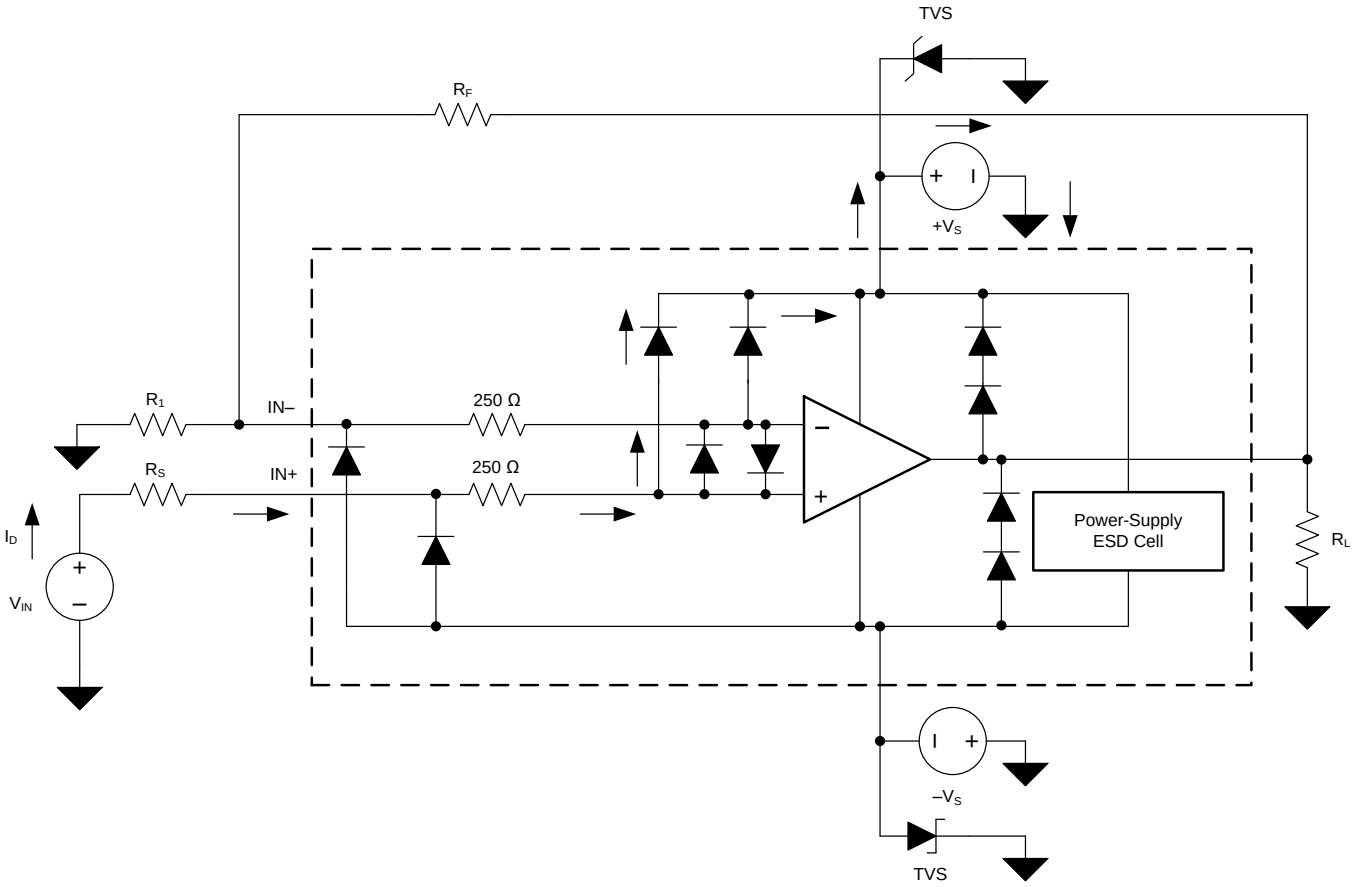



**Figure 48. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA168x but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (Figure 48), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 48 shows a specific example where the input voltage ($V_{IN}$) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher $V_{IN}$. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, $V_{IN}$ can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ($+V_S$ or $–V_S$) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply pins; see Figure 48. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPA168x input pins are protected from excessive differential voltage with back-to-back diodes; see Figure 48. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPA168x. Figure 48 illustrates an example configuration that implements a current-limiting feedback resistor.

### 9.4.3 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPA168x is approximately 200 ns.

# 10 Applications and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The OPA168x family of amplifiers is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

## 10.2 Typical Application

This application example highlights only a few of the circuits where the OPA168x can be used.

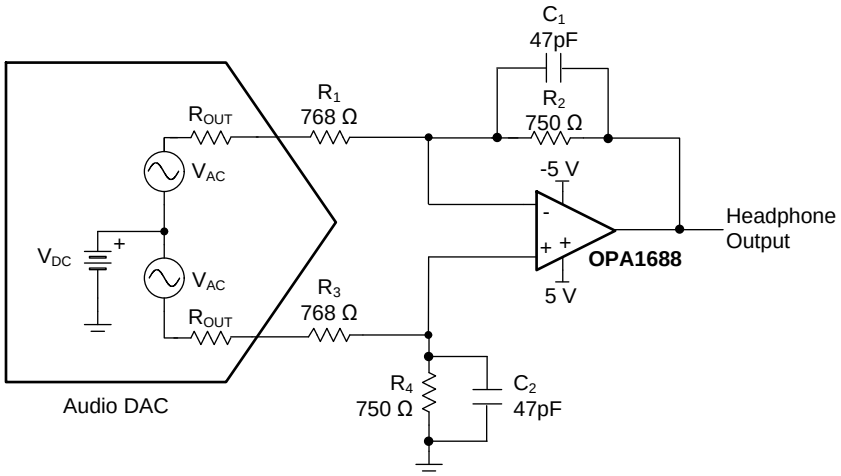



**Figure 49. Headphone Amplifier Circuit Configuration for Audio DACs that Output a Differential Voltage (Single Channel Shown)**

### 10.2.1 Design Requirements

The design requirements are:

- Supply voltage: 10 V (±5 V)
- Headphone loads: 16 Ω to 600 Ω
- THD+N: > 100 dB (1-kHz fundamental, 1 $V_{RMS}$ in 32 Ω, 22.4-kHz measurement bandwidth)
- Output power (before clipping): 50 mW into 32 Ω

## Typical Application (continued)

### 10.2.2 Detailed Design Procedure

The OPA168x family offers an excellent combination of specifications for headphone amplifier circuits (such as low noise, low distortion, capacitive load stability, and relatively high output current). Furthermore, the low-power supply current and small package options make the OPA1688 an exceptionally good choice for headphone amplifiers in portable devices. A common headphone amplifier circuit for audio digital-to-analog converters (DACs) with differential voltage outputs is illustrated in Figure 49. This circuit converts the differential voltage output of the DAC to a single-ended, ground-referenced signal and provides the additional current necessary for low-impedance headphones. For $R_2 = R_4$ and $R_1 = R_3$, the output voltage of the circuit is given by Equation 1:

$$V_{OUT} = 2 \times V_{AC} \frac{R_2}{R_1 + R_{OUT}} \quad (1)$$

where

- $R_{OUT}$ is the output impedance of the DAC and
- $2 \times V_{AC}$ is the unloaded differential output voltage

The output voltage required for headphones depends on the headphone impedance as well as the headphone efficiency. Both values can be provided by the headphone manufacturer, with headphone efficiency usually given as a sound pressure level (SPL) produced with 1 mW of input power and denoted by the Greek letter η. The SPL at other input power levels can be calculated from the efficiency specification using Equation 2:

$$\text{SPL (dB)} = \eta + 10 \log\left(\frac{P_{IN}}{1\ \text{mW}}\right) \quad (2)$$

Note that at extremely high power levels, the accuracy of this calculation decreases as a result of secondary effects in the headphone drivers. Figure 50 allows the SPL produced by a pair of headphones of a known sensitivity to be estimated for a given input power.

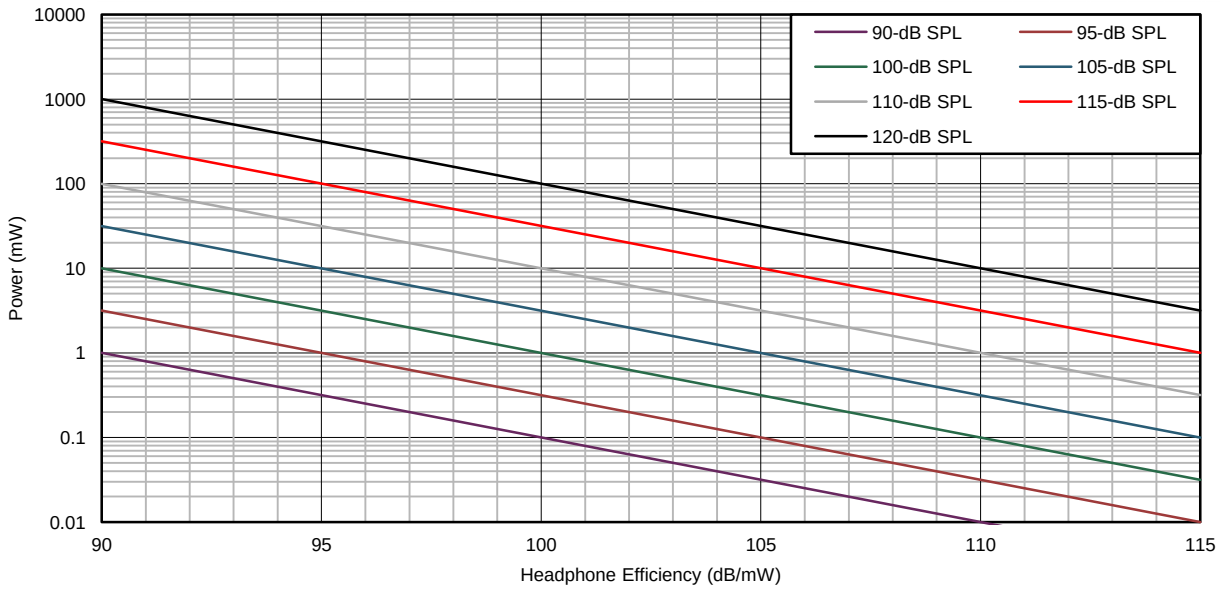



**Figure 50. SPLs Produced for Various Headphone Efficiencies and Input Power Levels**

## Typical Application (continued)

For example, a pair of headphones with a 95-dB/mW sensitivity given a 3-mW input signal produces a 100-dB SPL. If these headphones have a nominal impedance of 32 Ω, then the voltage and current from the headphone amplifier is as described in Equation 3 and Equation 4, respectively:

$$V = \sqrt{P_{IN} \times R_{HP}} = \sqrt{3\ mW \times 32\ \Omega} = 310\ mV_{RMS} \quad (3)$$

$$I = \sqrt{\frac{P_{IN}}{R_{HP}}} = \sqrt{\frac{3\ mW}{32\ \Omega}} = 9.68\ mA_{RMS} \quad (4)$$

Headphones can present a capacitive load at high frequencies that can destabilize the headphone amplifier circuit. Many headphone amplifiers use a resistor in series with the output to maintain stability; however this solution also compromises audio quality. The OPA168x family is able to maintain stability into large capacitive loads; therefore, a series output resistor is not necessary in the headphone amplifier circuit. TINA-TI™ simulations illustrate that the circuit in Figure 49 has a phase margin of approximately 50 degrees with a 400-pF load connected directly to the amplifier output.

### 10.2.3 Application Curves

The headphone amplifier circuit in Figure 49 is tested with three common headphone impedances: 16 Ω, 32 Ω, and 600 Ω. The total harmonic distortion and noise (THD+N) for increasing output voltages is given in Figure 51. This measurement is performed with a 1-kHz input signal and a measurement bandwidth of 22.4 kHz. The maximum output power and THD+N before clipping are given in Table 4. The maximum output power into low-impedance headphones is limited by the output current capabilities of the amplifier. For high-impedance headphones (600 Ω), the output voltage capabilities of the amplifier are the limiting factor. The circuit in Figure 49 is tested using ±5-V supplies that are common in many portable systems. However, using higher supply voltages increases the output power into 600-Ω headphones.

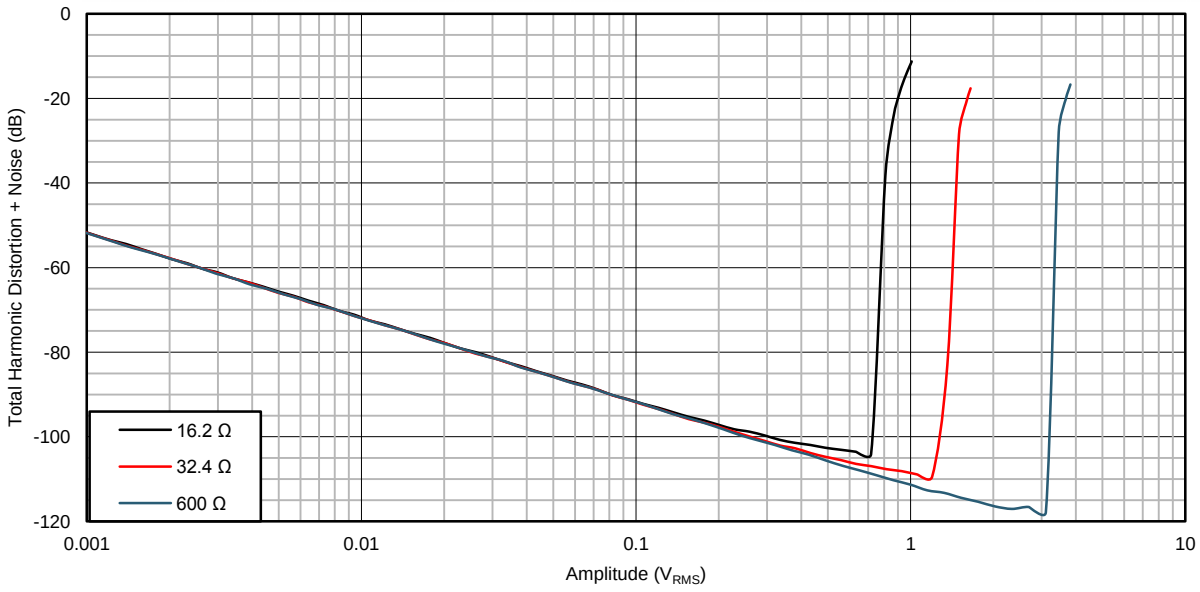



**Figure 51. THD+N for Increasing Output Voltages Into Three Load Impedances (Input Signal = 1 kHz, Measurement Bandwidth = 22.4 kHz)**

## Typical Application (continued)

**Table 4. Maximum Output Power and THD+N Before Clipping for Different Load Impedances**

| LOAD IMPEDANCE (Ω) | MAXIMUM OUTPUT POWER BEFORE CLIPPING (mW) | THD+N AT MAXIMUM OUTPUT POWER (dB) |
|---|---|---|
| 16 | 32 | –104.1 |
| 32 | 50 | –109.5 |
| 600 | 16 | –117.8 |

Figure 52, Figure 53, and Figure 54 further illustrate the exceptional performance of the OPA1688 as a headphone amplifier.

Figure 52 shows the THD+N over frequency for a 500-$mV_{RMS}$ output signal into the same three load impedances previously tested.

Figure 53 and Figure 54 show the output spectrum of the OPA1688 at low (1 mW) and high (50 mW) output power levels into a 32-Ω load. The distortion harmonics in both cases are approximately 120 dB below the fundamental.

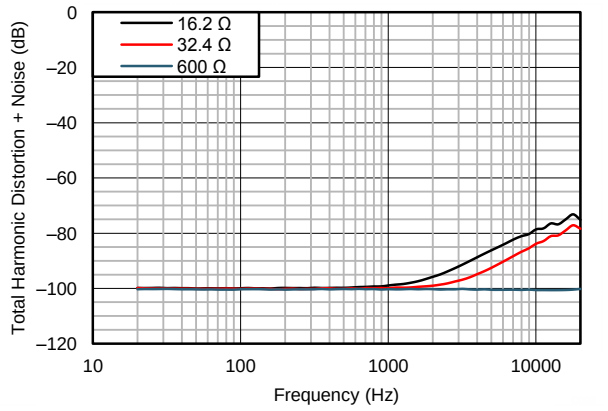



**Figure 52. THD+N Measured over Frequency (90-kHz Measurement Bandwidth) for a 500-$mV_{RMS}$ Output Level**

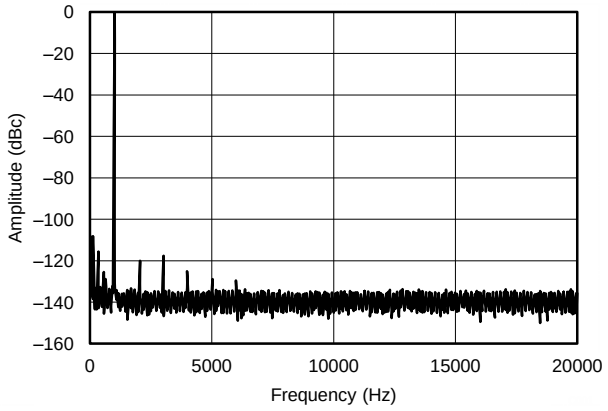



**Figure 53. Output Spectrum of a 1-mW, 1-kHz Tone into a 32-Ω Load (The third harmonic is dominant at a level of –117.6 dB relative to the fundamental.)**

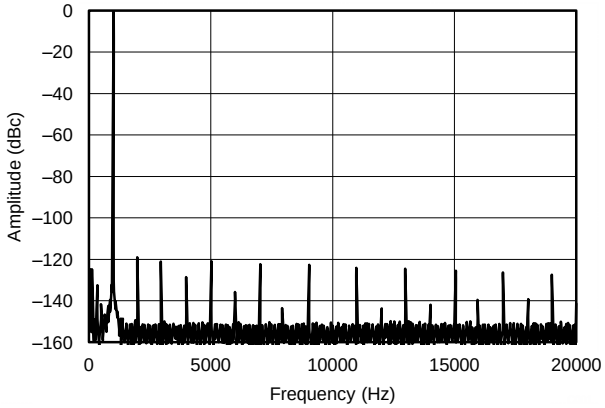



**Figure 54. Output Spectrum of a 50-mW, 1-kHz Tone Into a 32-Ω Load, Immediately Below the Onset of Clipping (The highest harmonic is the second harmonic at –119 dB below the fundamental.)**

# 11 Power Supply Recommendations

The OPA168x is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

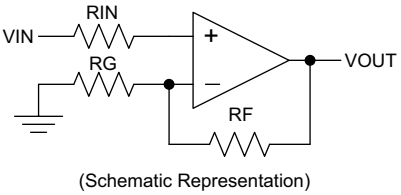
# 12 Layout

## 12.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 55, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 12.2 Layout Example



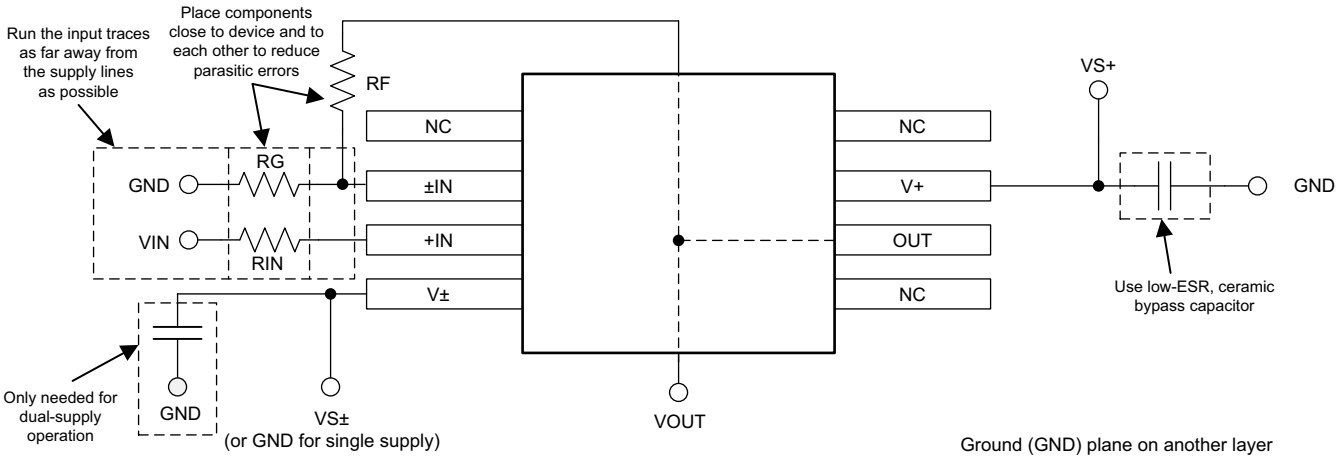




**Figure 55. Operational Amplifier Board Layout for a Noninverting Configuration**

# 13 Device and Documentation Support

## 13.1 Device Support

### 13.1.1 Development Support

#### *13.1.1.1 TINA-TI™ (Free Software Download)*

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

**NOTE**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

## 13.2 Documentation Support

### 13.2.1 Related Documentation

SBOA015 (AB-028) — *Feedback Plots Define Op Amp AC Performance*

SBOA128 — *EMI Rejection Ratio of Operational Amplifiers*

SLOA089 — *Circuit Board Layout Techniques*

SLOD006 — *Op Amps for Everyone*

TIPD128 — *Capacitive Load Drive Solution using an Isolation Resistor*

## 13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 5. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| OPA1688 | Click here | Click here | Click here | Click here | Click here |
| OPA1689 | Click here | Click here | Click here | Click here | Click here |

## 13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 13.5 Trademarks

E2E is a trademark of Texas Instruments.
SoundPlus is a trademark of Texas Instruments, Inc.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Blu-Ray is a trademark of Blu-ray Disc Association (BDA).
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

### 13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA1688ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | O1688A | Samples |
| OPA1688IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | O1688A | Samples |
| OPA1688IDRGR | ACTIVE | SON | DRG | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OP1688 | Samples |
| OPA1688IDRGT | ACTIVE | SON | DRG | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | OP1688 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

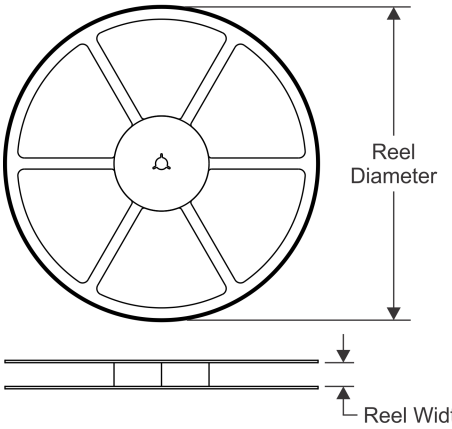
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

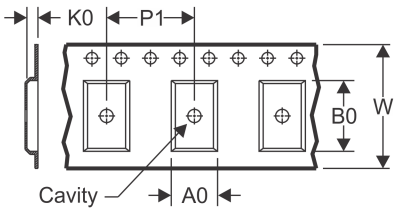
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

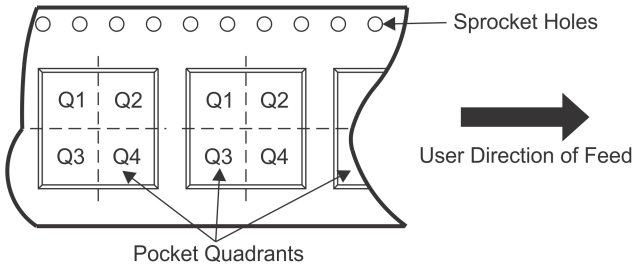



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

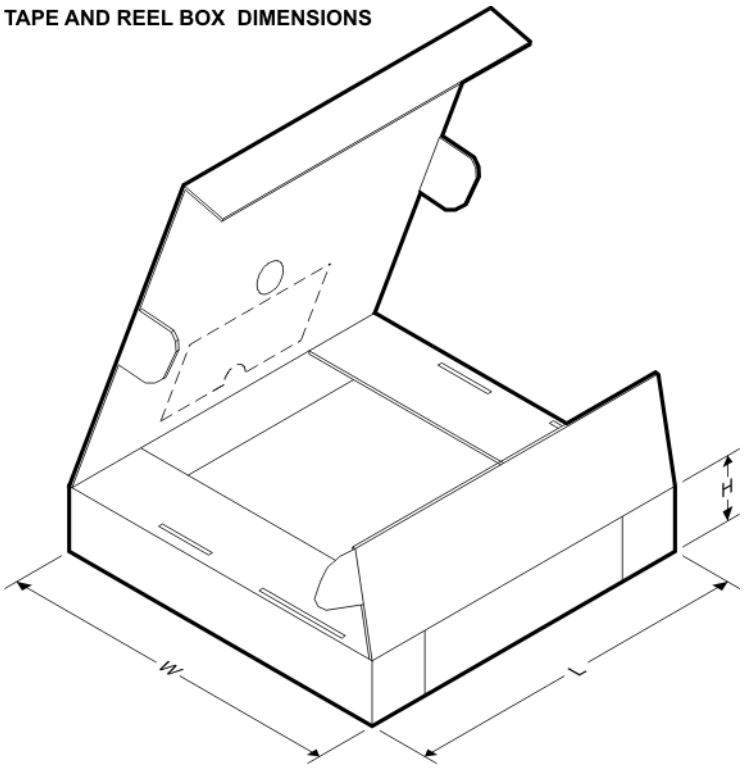
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA1688IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA1688IDRGR | SON | DRG | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| OPA1688IDRGT | SON | DRG | 8 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

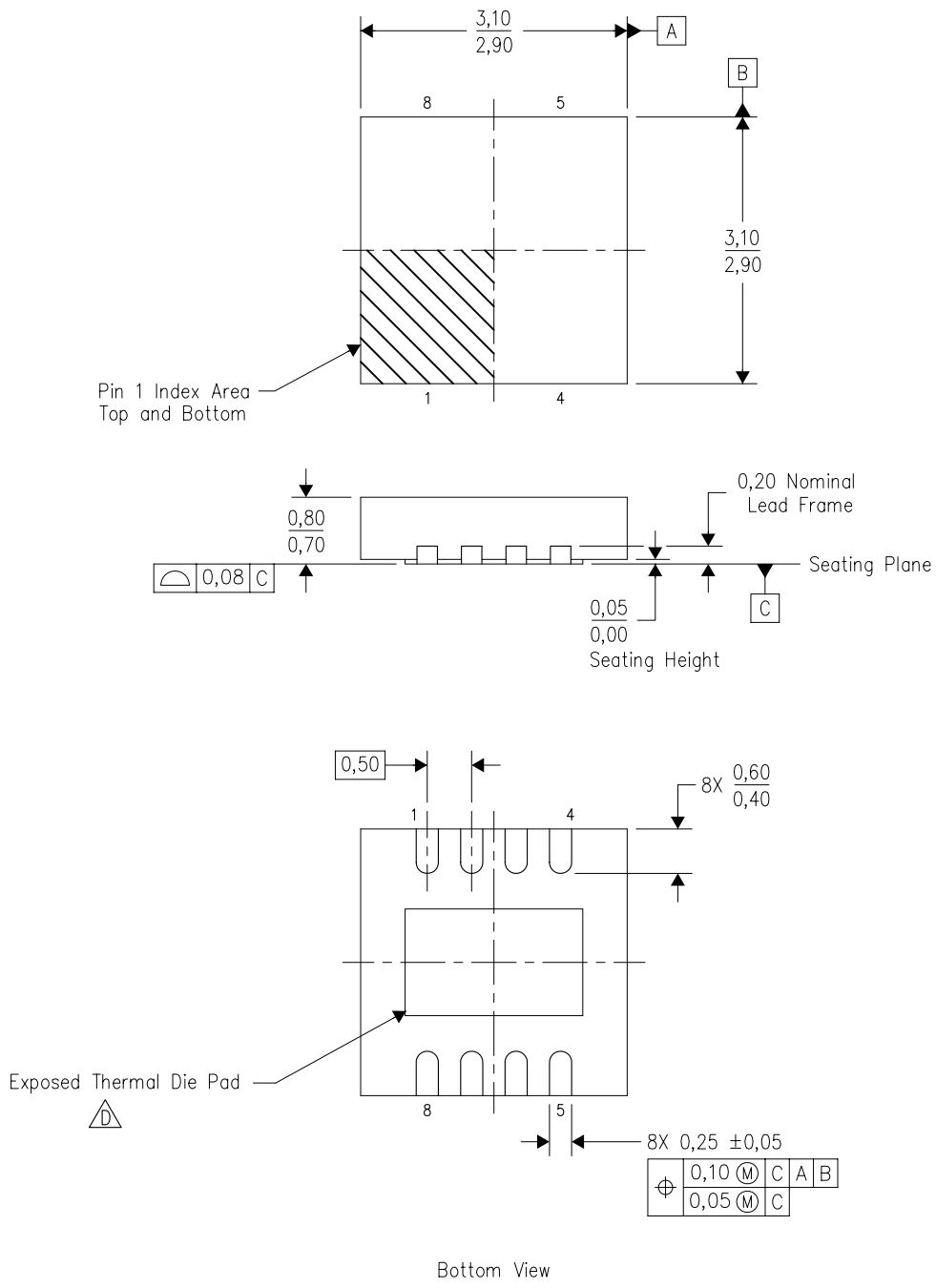
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA1688IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| OPA1688IDRGR | SON | DRG | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| OPA1688IDRGT | SON | DRG | 8 | 250 | 210.0 | 185.0 | 35.0 |

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

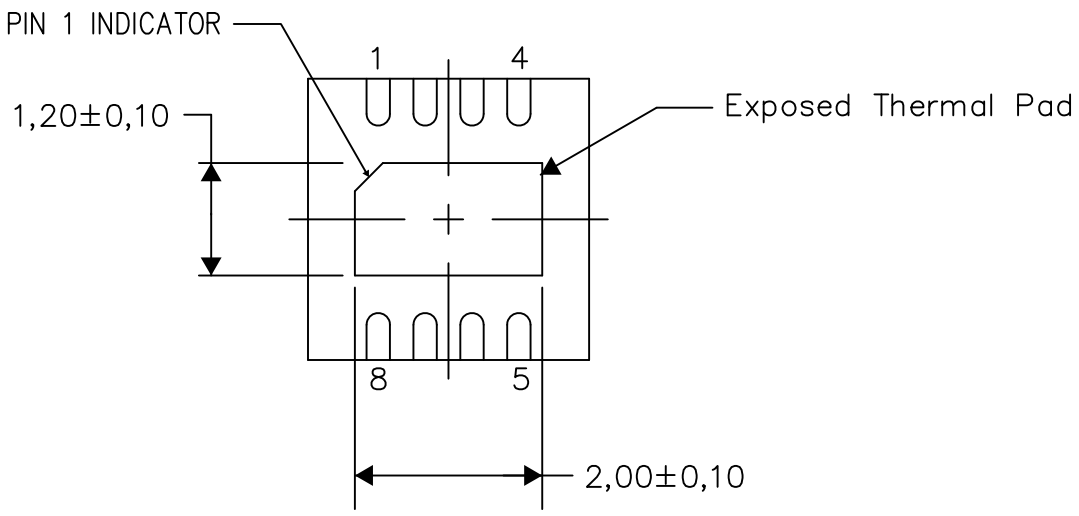
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



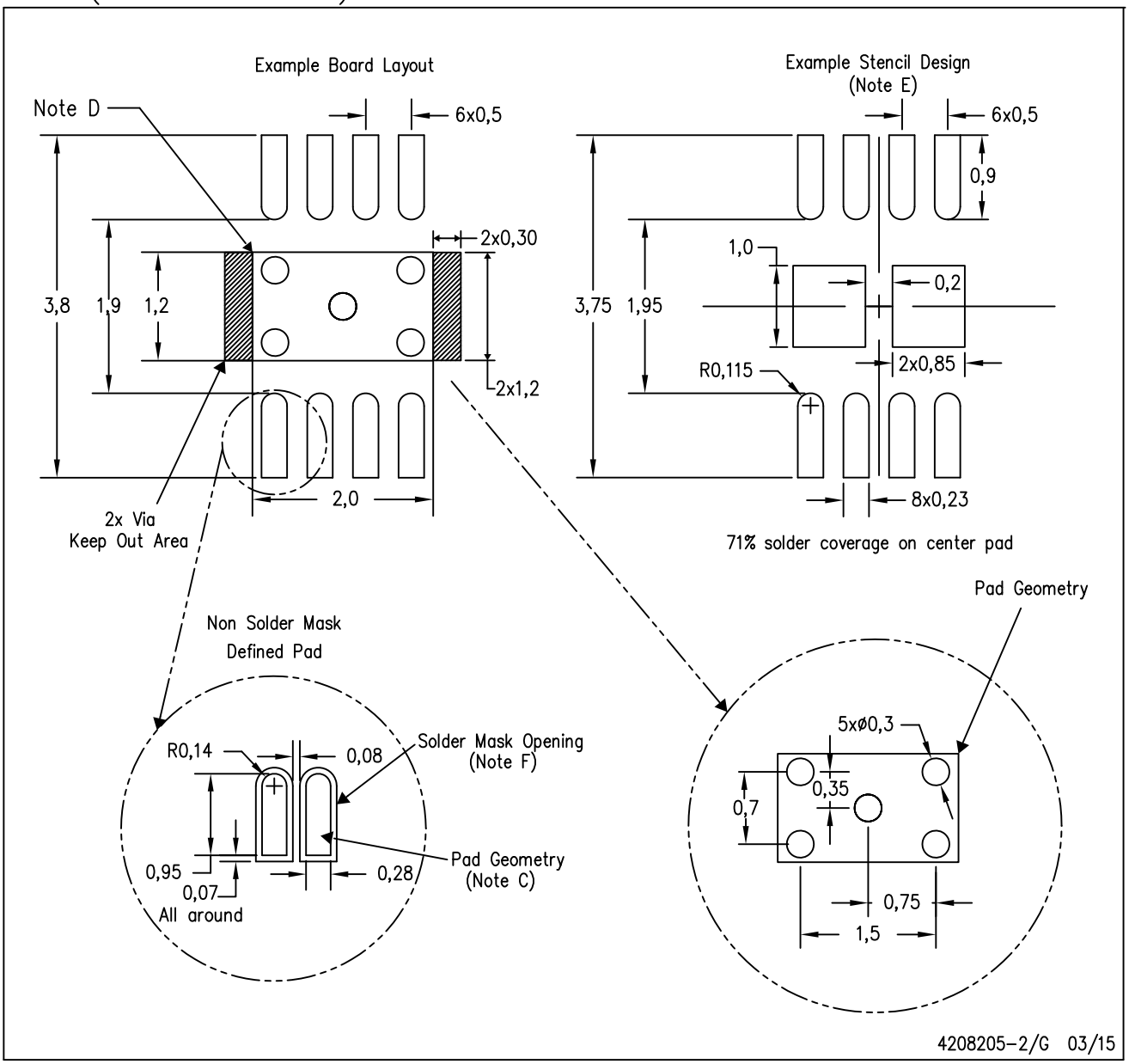

Bottom View

Exposed Thermal Pad Dimensions

4206881–2/I 03/15

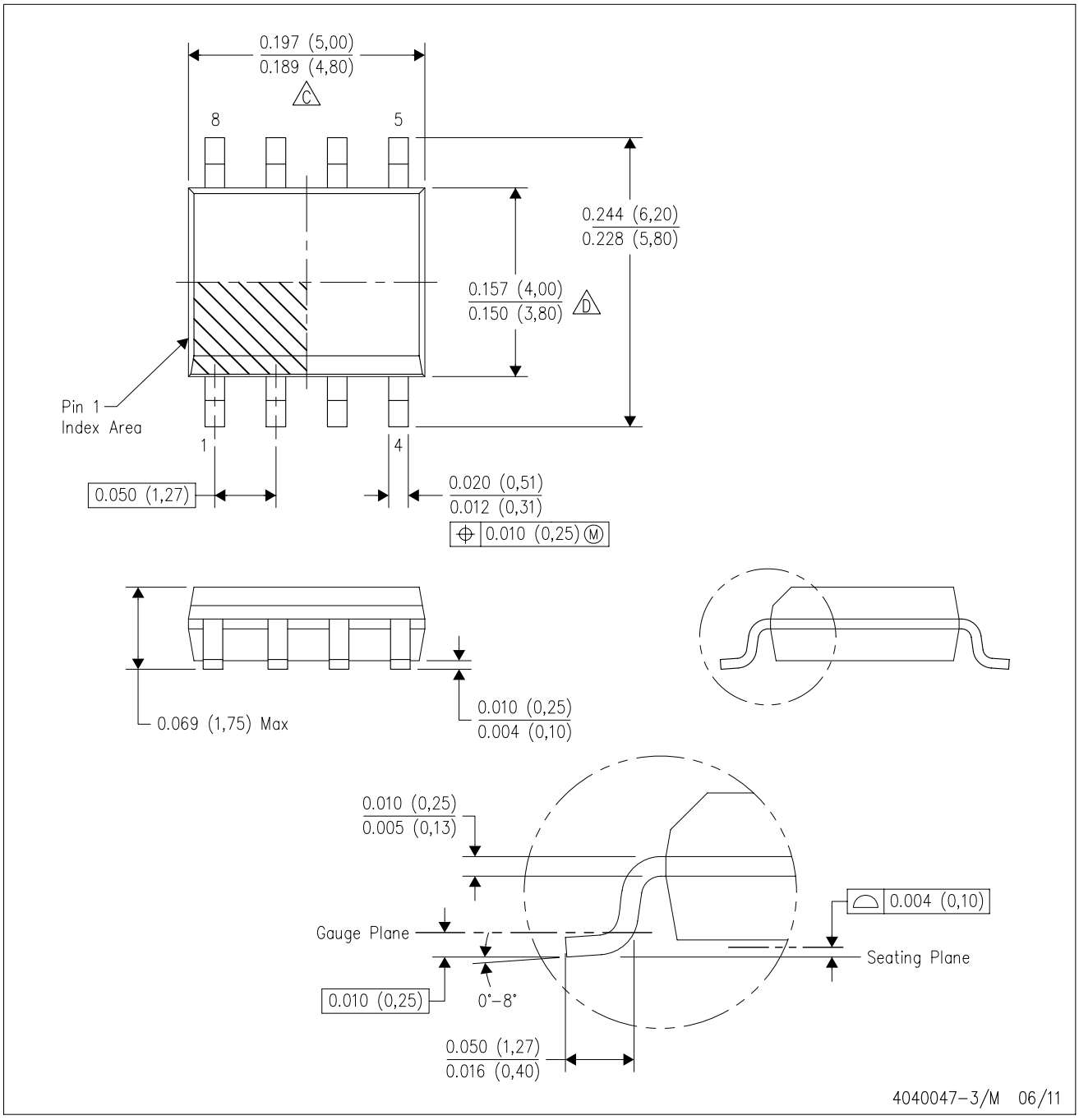
NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



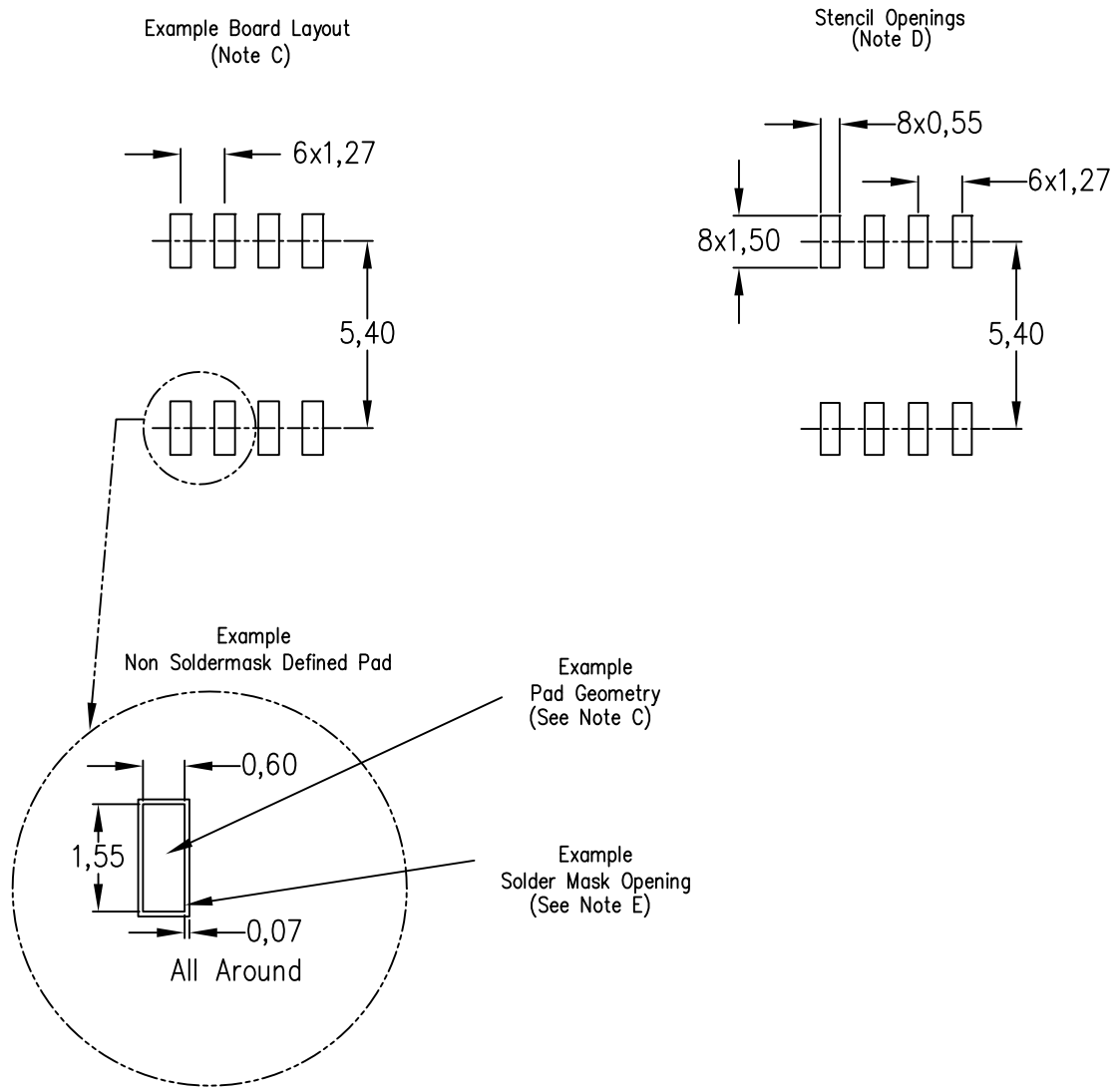

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TEXAS INSTRUMENTS

TL081, TL081A, TL081B, TL082, TL082A
TL082B, TL084, TL084A, TL084B

SLOS081I – FEBRUARY 1977 – REVISED MAY 2015

# TL08xx JFET-Input Operational Amplifiers

## 1 Features

- Low Power Consumption: 1.4 mA/ch Typical
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias Current: 30 pA Typical
- Low Input Offset Current: 5 pA Typical
- Output Short-Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typical
- High Input Impedance: JFET Input Stage
- Latch-Up-Free Operation
- High Slew Rate: 13 V/μs Typical
- Common-Mode Input Voltage Range Includes $V_{CC+}$

## 2 Applications

- Tablets
- White goods
- Personal electronics
- Computers

## 3 Description

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient.

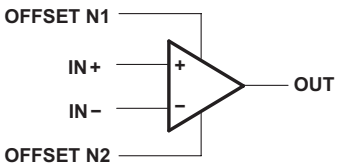
**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TL084xD | SOIC (14) | 8.65 mm × 3.91 mm |
| TL08xxFK | LCCC (20) | 8.89 mm × 8.89 mm |
| TL084xJ | CDIP (14) | 19.56 mm × 6.92 mm |
| TL084xN | PDIP (14) | 19.3 mm × 6.35 mm |
| TL084xNS | SO (14) | 10.3 mm × 5.3 mm |
| TL084xPW | TSSOP (14) | 5.0 mm × 4.4 mm |

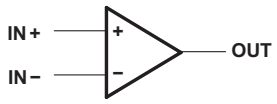
(1) For all available packages, see the orderable addendum at the end of the data sheet.

**Schematic Symbol**

TL081




TL082 (EACH AMPLIFIER)
TL084 (EACH AMPLIFIER)



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision H (January 2014) to Revision I** — **Page**

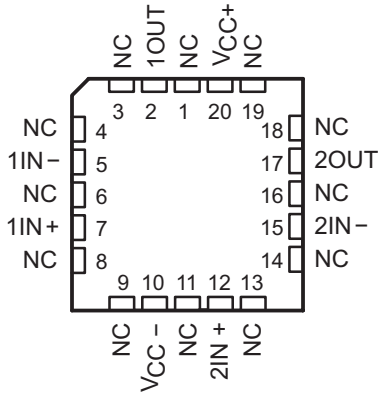
- Added *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Applications* ... 1
- Moved *Typical Characteristics* into *Specifications* section. ... 9

**Changes from Revision G (September 2004) to Revision H** — **Page**

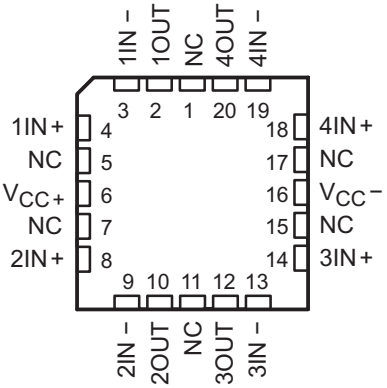
- Updated document to new TI data sheet format - no specification changes. ... 1
- Deleted *Ordering Information* table. ... 1

# 5 Pin Configuration and Functions

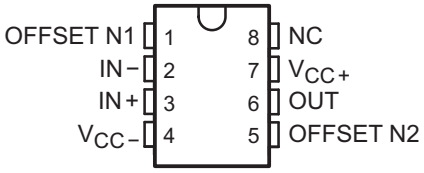
**TL082 FK Package**
**20-Pin LCCC**
**Top View**



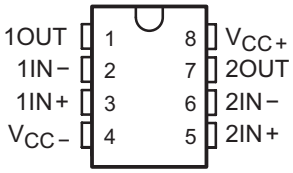

**TL084 FK Package**
**20-Pin LCCC**
**Top View**



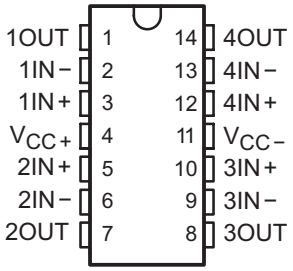

**TL081 and TL081x D, P, and PS Package**
**8-Pin SOIC, PDIP, and SO**
**Top View**




**TL082 and TL082x D, JG, P, PS and PW Package**
**8-Pin SOIC, CDIP, PDIP, SO, and TSSOP**
**Top View**




**TL084 and TL084x D, J, N, NS and PW Package**
**14-Pin SOIC, CDIP, PDIP, SO, and TSSOP**
**Top View**




**Pin Functions**

| PIN | | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| NAME | TL081 | TL082 | | TL084 | | | |
| | SOIC, PDIP, SO | SOIC, CDIP, PDIP, SO, TSSOP | LCCC | SOIC, CDIP, PDIP, SO, TSSOP | LCCC | | |
| 1IN– | — | 2 | 5 | 2 | 3 | I | Negative input |
| 1IN+ | — | 3 | 7 | 3 | 4 | I | Positive input |
| 1OUT | — | 1 | 2 | 1 | 2 | O | Output |
| 2IN– | — | 6 | 15 | 6 | 9 | I | Negative input |
| 2IN+ | — | 5 | 12 | 5 | 8 | I | Positive input |
| 2OUT | — | 7 | 17 | 7 | 10 | O | Output |
| 3IN– | — | — | — | 9 | 13 | I | Negative input |
| 3IN+ | — | — | — | 10 | 14 | I | Positive input |
| 3OUT | — | — | — | 8 | 12 | O | Output |
| 4IN– | — | — | — | 13 | 19 | I | Negative input |
| 4IN+ | — | — | — | 12 | 18 | I | Positive input |
| 4OUT | — | — | — | 14 | 20 | O | Output |

## Pin Functions (continued)

| PIN | | | | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| NAME | TL081 | TL082 | | TL084 | | | |
| | SOIC, PDIP, SO | SOIC, CDIP, PDIP, SO, TSSOP | LCCC | SOIC, CDIP, PDIP, SO, TSSOP | LCCC | | |
| IN– | 2 | — | — | — | — | I | Negative input |
| IN+ | 3 | — | — | — | — | I | Positive input |
| NC | 8 | — | 1 | — | 1 | — | Do not connect |
| | | | 3 | | | | |
| | | | 4 | | 5 | | |
| | | | 6 | | | | |
| | | | 8 | | 7 | | |
| | | | 9 | | | | |
| | | | 11 | | 11 | | |
| | | | 13 | | | | |
| | | | 14 | | 15 | | |
| | | | 16 | | | | |
| | | | 18 | | 17 | | |
| OFFSET N1 | 1 | — | — | — | — | — | Input offset adjustment |
| OFFSET N2 | 5 | — | — | — | — | — | Input offset adjustment |
| OUT | 6 | — | — | — | — | O | Output |
| $V_{CC-}$ | 4 | 4 | 10 | 11 | 16 | — | Power supply |
| $V_{CC+}$ | 7 | 8 | 20 | 4 | 6 | — | Power supply |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC+}$ | Supply voltage(2) | | | | 18 | V |
| $V_{CC-}$ | | | | | –18 | |
| $V_{ID}$ | Differential input voltage(3) | | | | ±30 | V |
| $V_I$ | Input voltage(2)(4) | | | | ±15 | V |
| | Duration of output short circuit(5) | | | Unlimited | | |
| | Continuous total power dissipation | | | See *Dissipation Rating Table* | | |
| $T_A$ | Operating free-air temperature | | TL08_C<br>TL08_AC<br>TL08_BC | 0 | 70 | °C |
| | | | TL08_I | –40 | 85 | |
| | | | TL084Q | –40 | 125 | |
| | | | TL08_M | –55 | 125 | |
| | Operating virtual junction temperature | | | | 150 | °C |
| $T_C$ | Case temperature for 60 seconds | FK package | TL08_M | | 260 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | J or JG package | TL08_M | | 300 | °C |
| $T_{stg}$ | Storage temperature | | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between $V_{CC+}$ and $V_{CC-}$.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | 1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | 1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC+}$ | Supply voltage | | 5 | 15 | V |
| $V_{CC-}$ | Supply voltage | | –5 | –15 | V |
| $V_{CM}$ | Common-mode voltage | | $V_{CC-}$ + 4 | $V_{CC+}$ – 4 | V |
| $T_A$ | Ambient temperature | TL08xM | –55 | 125 | °C |
| | | TL08xQ | –40 | 125 | |
| | | TL08xI | –40 | 85 | |
| | | TL08xC | 0 | 70 | |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TL08xx | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | D (SOIC) | | N (PDIP) | NS (SO) | P (PDIP) | PS (SO) | PW (TSSOP) | | |
| | | 8 PINS | 14 PINS | 14 PINS | 14 PINS | {PIN COUNT} PINS | {PIN COUNT} PINS | 8 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[2][3] | 97 | 86 | 76 | 80 | 85 | 95 | 149 | 113 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / R_{\theta JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## 6.5 Electrical Characteristics for TL08xC, TL08xxC, and TL08xI

$V_{CC±}$ = ±15 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$[1] | TL081C, TL082C, TL084C | | | TL081AC, TL082AC, TL084AC | | | TL081BC, TL082BC, TL084BC | | | TL081I, TL082I, TL084I | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_O$ = 0, $R_S$ = 50 Ω | 25°C | | 3 | 15 | | 3 | 6 | | 2 | 3 | | 3 | 6 | mV |
| | | | Full range | | | 20 | | | 7.5 | | | 5 | | | 9 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | $V_O$ = 0, $R_S$ = 50 Ω | Full range | | 18 | | | 18 | | | 18 | | | 18 | | µV/°C |
| $I_{IO}$ | Input offset current[2] | $V_O$ = 0 | 25°C | | 5 | 200 | | 5 | 100 | | 5 | 100 | | 5 | 100 | pA |
| | | | Full range | | | 2 | | | 2 | | | 2 | | | 10 | nA |
| $I_{IB}$ | Input bias current[2] | $V_O$ = 0 | 25°C | | 30 | 400 | | 30 | 200 | | 30 | 200 | | 30 | 200 | pA |
| | | | Full range | | | 10 | | | 7 | | | 7 | | | 20 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | ±11 | –12 to 15 | | ±11 | –12 to 15 | | ±11 | –12 to 15 | | ±11 | –12 to 15 | | V |
| $V_{OM}$ | Maximum peak output voltage swing | $R_L$ = 10 kΩ | 25°C | ±12 | ±13.5 | | ±12 | ±13.5 | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| | | $R_L$ ≥ 10 kΩ | Full range | ±12 | | | ±12 | | | ±12 | | | ±12 | | | |
| | | $R_L$ ≥ 2 kΩ | | ±10 | ±12 | | ±10 | ±12 | | ±10 | ±12 | | ±10 | ±12 | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_O$ = ±10 V, $R_L$ ≥ 2 kΩ | 25°C | 25 | 200 | | 50 | 200 | | 50 | 200 | | 50 | 200 | | V/mV |
| | | | Full range | 15 | | | 15 | | | 25 | | | 25 | | | |
| $B_1$ | Unity-gain bandwidth | | 25°C | | 3 | | | 3 | | | 3 | | | 3 | | MHz |
| $r_i$ | Input resistance | | 25°C | | $10^{12}$ | | | $10^{12}$ | | | $10^{12}$ | | | $10^{12}$ | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min, $V_O$ = 0, $R_S$ = 50 Ω | 25°C | 70 | 86 | | 75 | 86 | | 75 | 86 | | 75 | 86 | | dB |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{CC±}/\Delta V_{IO}$) | $V_{CC}$ = ±15 V to ±9 V, $V_O$ = 0, $R_S$ = 50 Ω | 25°C | 70 | 86 | | 80 | 86 | | 80 | 86 | | 80 | 86 | | dB |

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for $T_A$ is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and –40°C to 85°C for TL08_I.
(2) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

## Electrical Characteristics for TL08xC, TL08xxC, and TL08xI (continued)

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ (1) | TL081C, TL082C, TL084C | | | TL081AC, TL082AC, TL084AC | | | TL081BC, TL082BC, TL084BC | | | TL081I, TL082I, TL084I | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $I_{CC}$ | Supply current (each amplifier) | $V_O$ = 0, No load | 25°C | | 1.4 | 2.8 | | 1.4 | 2.8 | | 1.4 | 2.8 | | 1.4 | 2.8 | mA |
| $V_{O1}/V_{O2}$ | Crosstalk attenuation | $A_{VD}$ = 100 | 25°C | | 120 | | | 120 | | | 120 | | | 120 | | dB |

## 6.6 Electrical Characteristics for TL08xM and TL084x

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS (1) | $T_A$ | TL081M, TL082M | | | TL084Q, TL084M | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{IO}$ | Input offset voltage | $V_O$ = 0, $R_S$ = 50 Ω | 25°C | | 3 | 6 | | 3 | 9 | mV |
| | | | Full range | | | 9 | | | 15 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | $V_O$ = 0, $R_S$ = 50 Ω | Full range | | 18 | | | 18 | | µV/°C |
| $I_{IO}$ | Input offset current (2) | $V_O$ = 0 | 25°C | | 5 | 100 | | 5 | 100 | pA |
| | | | 125°C | | | 20 | | | 20 | nA |
| $I_{IB}$ | Input bias current (2) | $V_O$ = 0 | 25°C | | 30 | 200 | | 30 | 200 | pA |
| | | | 125°C | | | 50 | | | 50 | nA |
| $V_{ICR}$ | Common-mode input voltage range | | 25°C | ±11 | –12 to 15 | | ±11 | –12 to 15 | | V |
| $V_{OM}$ | Maximum peak output voltage swing | $R_L$ = 10 kΩ | 25°C | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| | | $R_L$ ≥ 10 kΩ | Full range | ±12 | | | ±12 | | | |
| | | $R_L$ ≥ 2 kΩ | | ±10 | ±12 | | ±10 | ±12 | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_O$ = ±10 V, $R_L$ ≥ 2 kΩ | 25°C | 25 | 200 | | 25 | 200 | | V/mV |
| | | | Full range | 15 | | | 15 | | | |
| $B_1$ | Unity-gain bandwidth | | 25°C | | 3 | | | 3 | | MHz |
| $r_i$ | Input resistance | | 25°C | | $10^{12}$ | | | $10^{12}$ | | Ω |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = $V_{ICR}$min, $V_O$ = 0, $R_S$ = 50 Ω | 25°C | 80 | 86 | | 80 | 86 | | dB |
| $k_{SVR}$ | Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$) | $V_{CC}$ = ±15 V to ±9 V, $V_O$ = 0, $R_S$ = 50 Ω | 25°C | 80 | 86 | | 80 | 86 | | dB |
| $I_{CC}$ | Supply current (each amplifier) | $V_O$ = 0, No load | 25°C | | 1.4 | 2.8 | | 1.4 | 2.8 | mA |
| $V_{O1}/V_{O2}$ | Crosstalk attenuation | $A_{VD}$ = 100 | 25°C | | 120 | | | 120 | | dB |

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 13. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

## 6.7 Operating Characteristics

$V_{CC\pm}$ = ±15 V, $T_A$= 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SR | Slew rate at unity gain | $V_I$ = 10 V, $R_L$ = 2 kΩ, $C_L$ = 100 pF, See Figure 19 | 8 (1) | 13 | | V/µs |
| | | $V_I$ = 10 V, $R_L$ = 2 kΩ, $C_L$ = 100 pF, $T_A$ = − 55°C to 125°C, See Figure 19 | 5 (1) | | | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## Operating Characteristics (continued)

$V_{CC\pm}$ = ±15 V, $T_A$= 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_r$ | Rise-time | $V_I$ = 20 V, $R_L$ = 2 kΩ, $C_L$ = 100 pF, See Figure 19 | | | 0.05 | | µs |
| | overshoot factor | | | | 20% | | |
| $V_n$ | Equivalent input noise voltage | $R_S$ = 20 Ω | f = 1 kHz | | 18 | | nV/√Hz |
| | | | f = 10 Hz to 10 kHz | | 4 | | µV |
| $I_n$ | Equivalent input noise current | $R_S$ = 20 Ω, | f = 1 kHz | | 0.01 | | pA/√Hz |
| THD | Total harmonic distortion | $V_I$rms = 6 V, $A_{VD}$ = 1, $R_S$ ≤ 1 kΩ, $R_L$ ≥ 2 kΩ, f = 1 kHz, | | | 0.003% | | |

## 6.8 Dissipation Rating Table

| PACKAGE | $T_A$ ≤ 25°C POWER RATING | DERATING FACTOR | DERATE ABOVE $T_A$ | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING | $T_A$ = 125°C POWER RATING |
|---|---|---|---|---|---|---|
| D (14 pin) | 680 mW | 7.6 mW/°C | 60°C | 604 m/W | 490 mW | 186 mW |
| FK | 680 mW | 11.0 mW/°C | 88°C | 680 m/W | 680 mW | 273 mW |
| J | 680 mW | 11.0 mW/°C | 88°C | 680 m/W | 680 mW | 273 mW |
| JG | 680 mW | 8.4 mW/°C | 69°C | 672 m/W | 546 mW | 210 mW |

## 6.9 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices. The Figure numbers referenced in the following graphs are located in *Parameter Measurement Information*.

**Table 1. Table of Graphs**

| | | | Figure |
|---|---|---|---|
| $V_{OM}$ | Maximum peak output voltage | versus Frequency<br>versus Free-air temperature<br>versus Load resistance<br>versus Supply voltage | Figure 1, Figure 2, Figure 3<br>Figure 4<br>Figure 5<br>Figure 6 |
| $A_{VD}$ | Large-signal differential voltage amplification | versus Free-air temperature<br>versus Load resistance | Figure 7<br>Figure 8 |
| | Differential voltage amplification | versus Frequency with feed-forward compensation | Figure 9 |
| $P_D$ | Total power dissipation | versus Free-air temperature | Figure 10 |
| $I_{CC}$ | Supply current | versus Free-air temperature<br>versus Supply voltage | Figure 11<br>Figure 12 |
| $I_{IB}$ | Input bias current | versus Free-air temperature | Figure 13 |
| | Large-signal pulse response | versus Time | Figure 14 |
| $V_O$ | Output voltage | versus Elapsed time | Figure 15 |
| CMRR | Common-mode rejection ratio | versus Free-air temperature | Figure 16 |
| $V_n$ | Equivalent input noise voltage | versus Frequency | Figure 17 |
| THD | Total harmonic distortion | versus Frequency | Figure 18 |

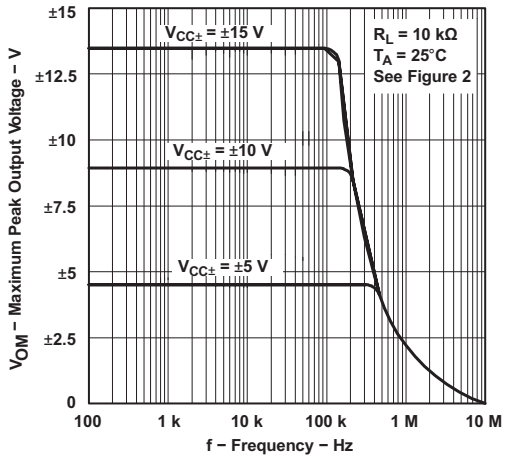



**Figure 1. Maximum Peak Output Voltage vs Frequency**

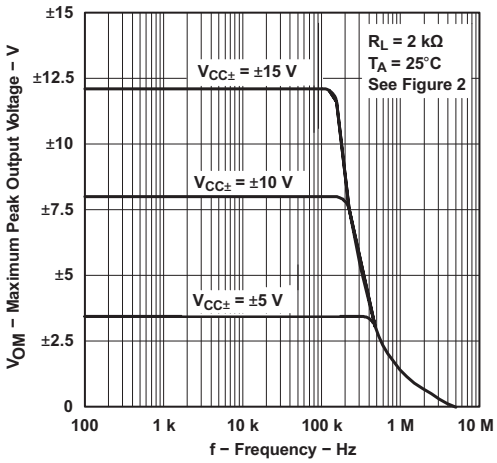



**Figure 2. Maximum Peak Output Voltage vs Frequency**

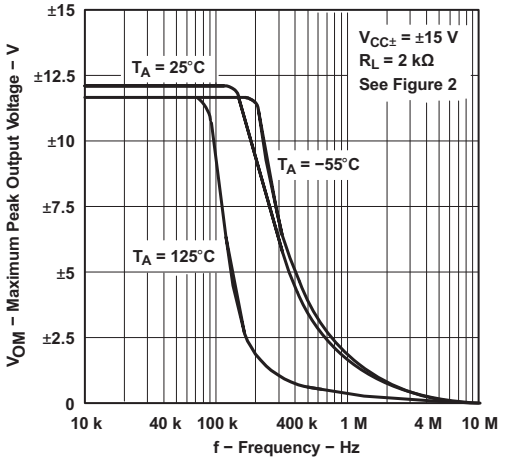



**Figure 3. Maximum Peak Voltage vs Frequency**

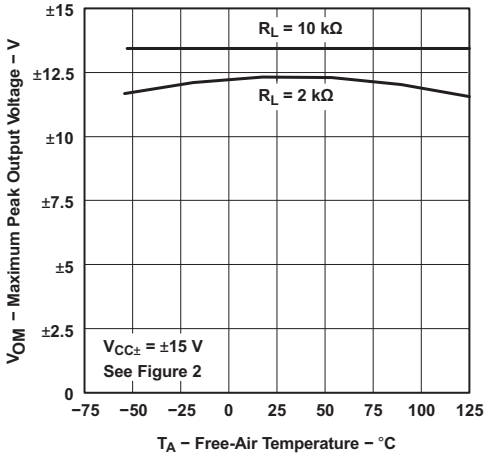



**Figure 4. Maximum Peak Output Voltage vs Free-Air Temperature**

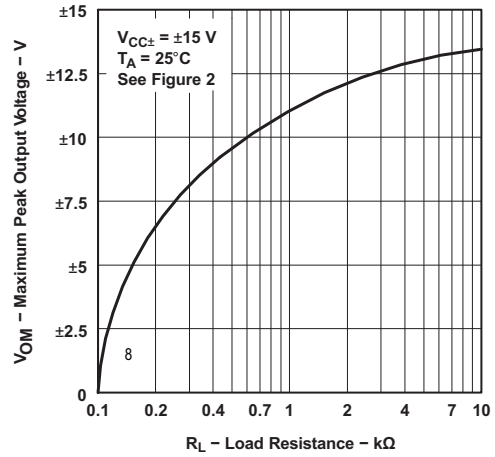



**Figure 5. Maximum Peak Output Voltage vs Load Resistance**

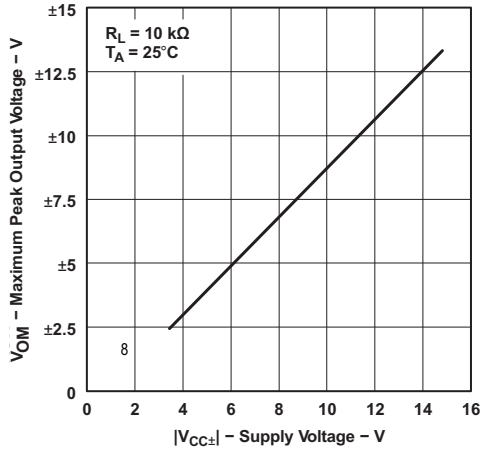



**Figure 6. Maximum Peak Output Voltage vs Supply Voltage**

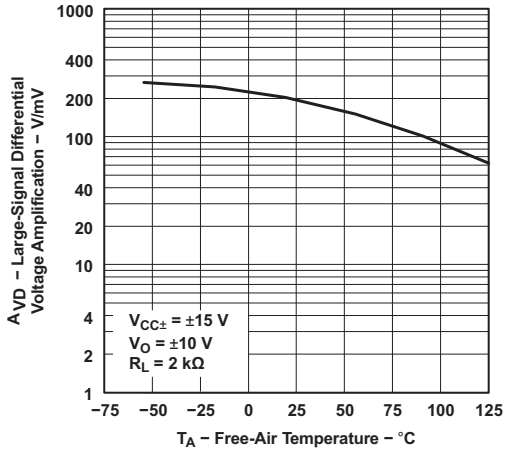



**Figure 7. Large-Signal Differential Voltage Amplification vs Free-Air Temperature**

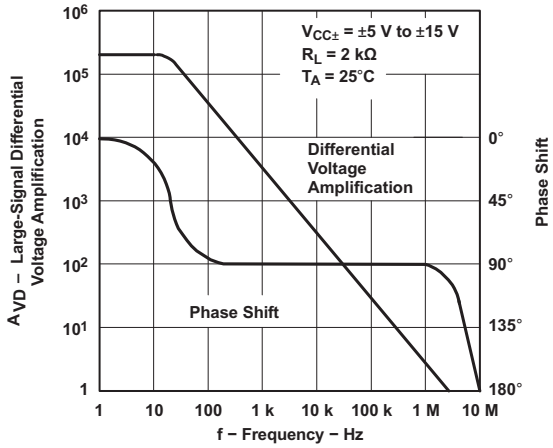



**Figure 8. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency**

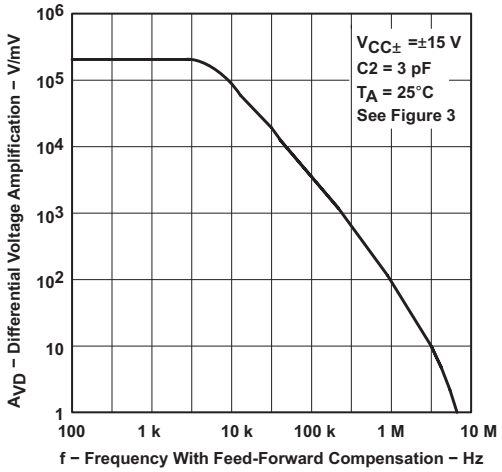



**Figure 9. Differential Voltage Amplification vs Frequency with Feed-Forward Compensation**

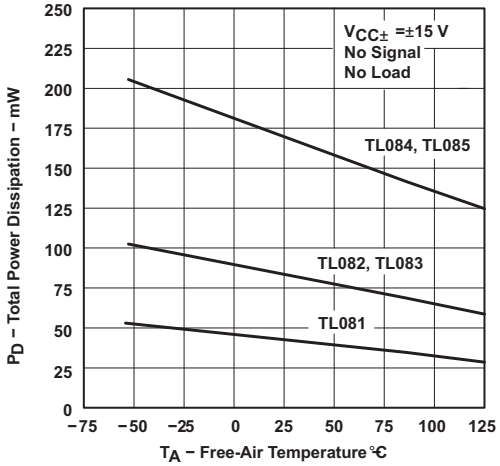



**Figure 10. Total Power Dissipation vs Free-Air Temperature**

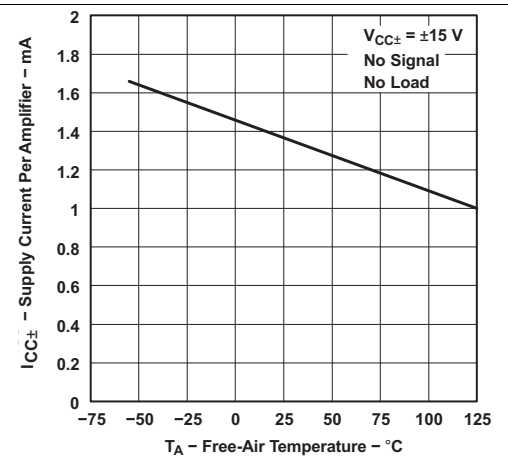



**Figure 11. Supply Current per Amplifier vs Free-Air Temperature**

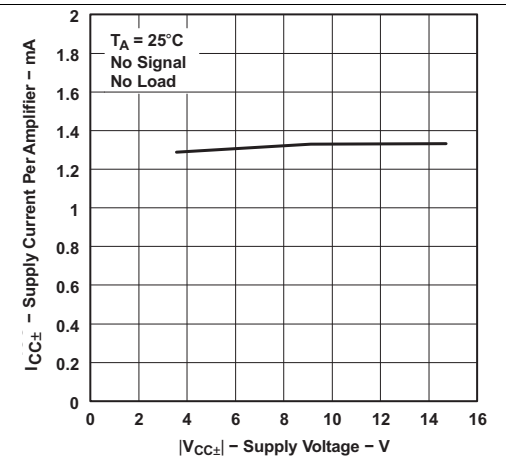



**Figure 12. Supply Current per Amplifier vs Supply Voltage**

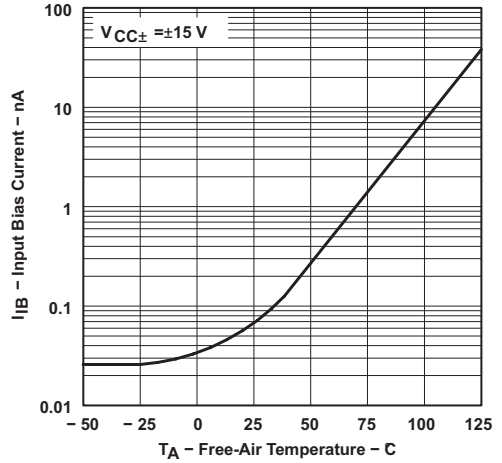



**Figure 13. Input Bias Current vs Free-Air Temperature**

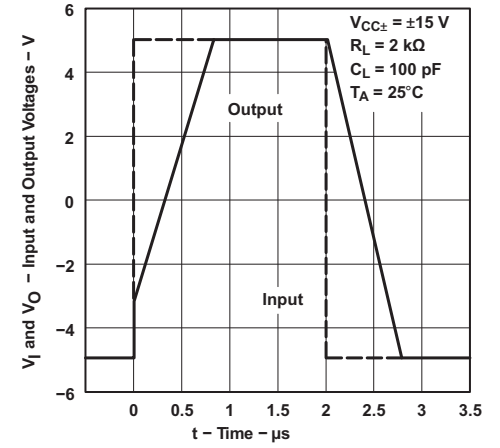



**Figure 14. Voltage-Follower Large-Signal Pulse Response**

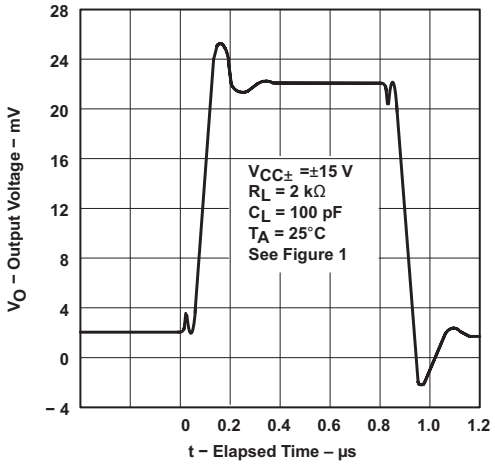



**Figure 15. Output Voltage vs Elapsed Time**

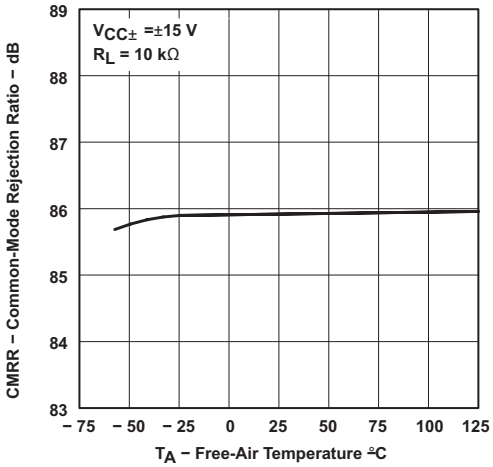



**Figure 16. Common-Mode Rejection Ratio vs Free-Air Temperature**

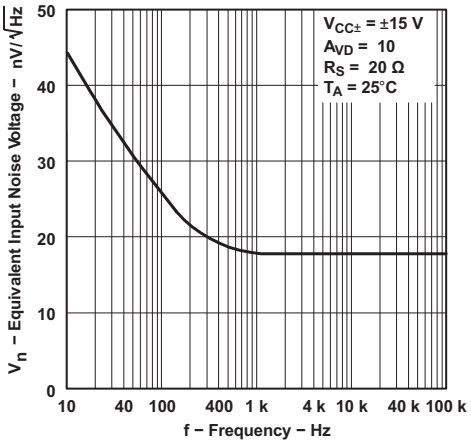



**Figure 17. Equivalent Input Noise Voltage vs Frequency**

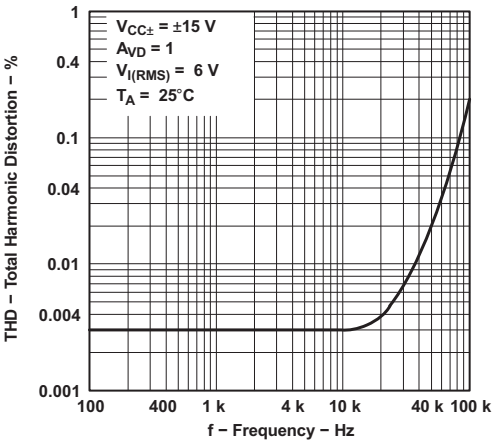



**Figure 18. Total Harmonic Distortion vs Frequency**

## 7 Parameter Measurement Information

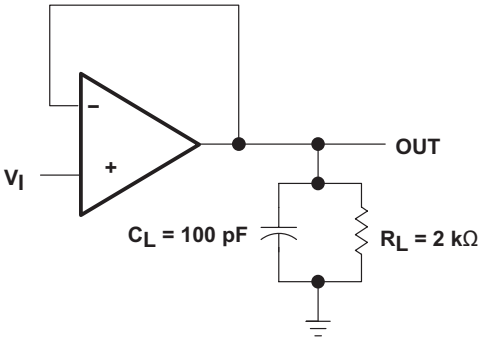



**Figure 19. Test Figure 1**

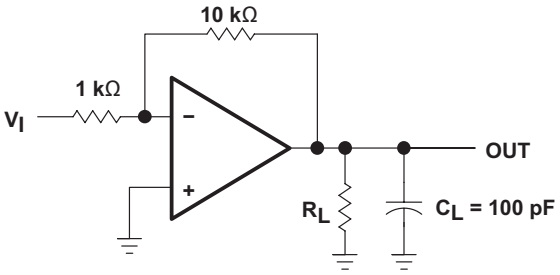



**Figure 20. Test Figure 2**

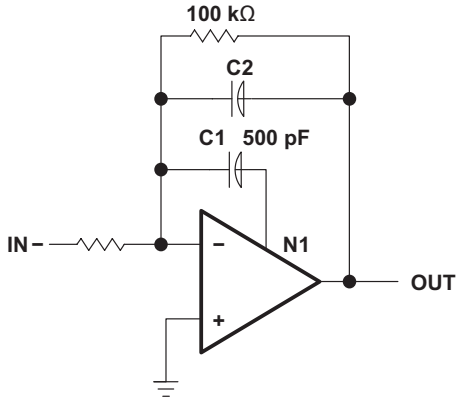



**Figure 21. Test Figure 3**

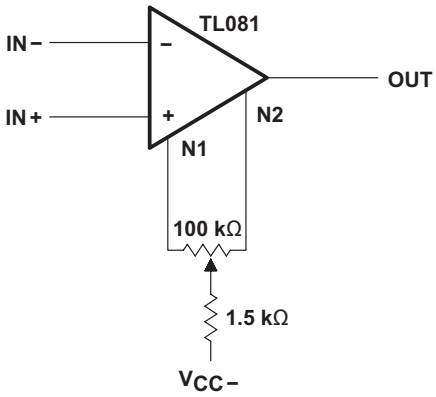



**Figure 22. Test Figure 4**

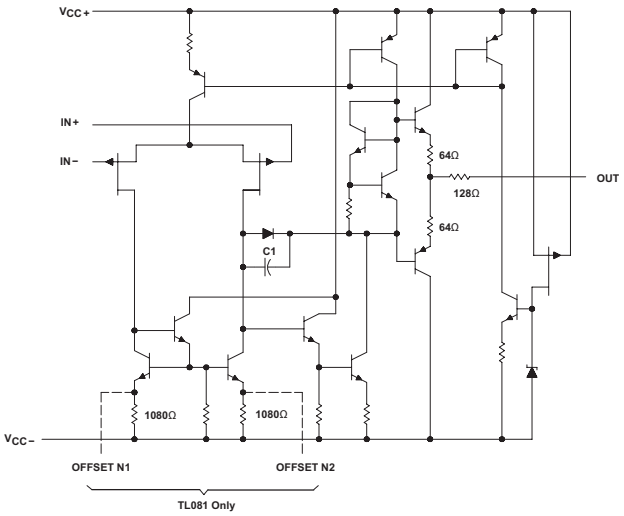
# 8 Detailed Description

## 8.1 Overview

The TL08xx JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08xx family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to +125°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to +125°C.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

### 8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL08x devices will add little harmonic distortion when used in audio signal applications.

### 8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 13-V/µs slew rate.

## 8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

# 9 Applications and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TL08x series of operational amplifiers can be used in countless applications. The few applications in this section show principles used in all applications of these parts.

## 9.2 Typical Applications

### 9.2.1 Inverting Amplifier Application

A typical application for an operational amplifier in an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

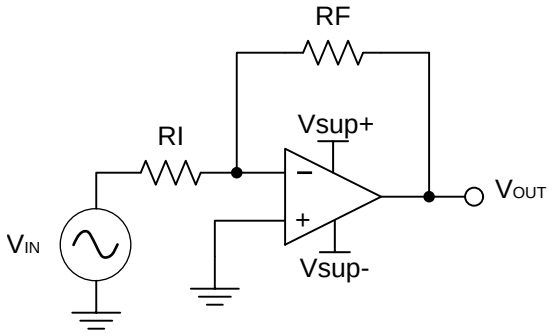



**Figure 23. Schematic for Inverting Amplifier Application**

#### *9.2.1.1 Design Requirements*

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

#### *9.2.1.2 Detailed Design Procedure*

Determine the gain required by the inverting amplifier:

$$A_v = \frac{VOUT}{VIN} \tag{1}$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

Once the desired gain is determined, choose a value for RI or RF. Choosing a value in the kΩ range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 kΩ for RI which means 36 kΩ will be used for RF. This was determined by Equation 3.

$$A_v = -\frac{RF}{RI} \tag{3}$$

## Typical Applications (continued)

### 9.2.1.3 Application Curve

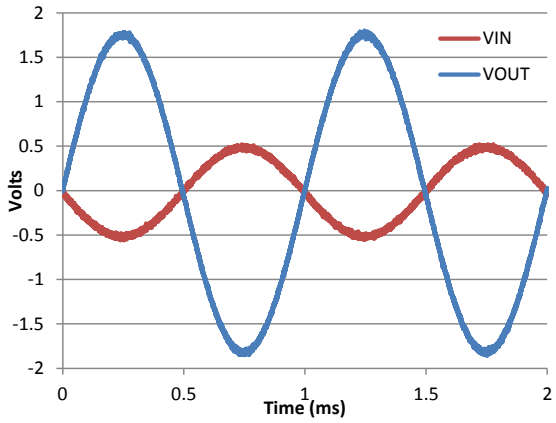



**Figure 24. Input and output voltages of the inverting amplifier**

## 9.3 System Examples

### 9.3.1 General Applications

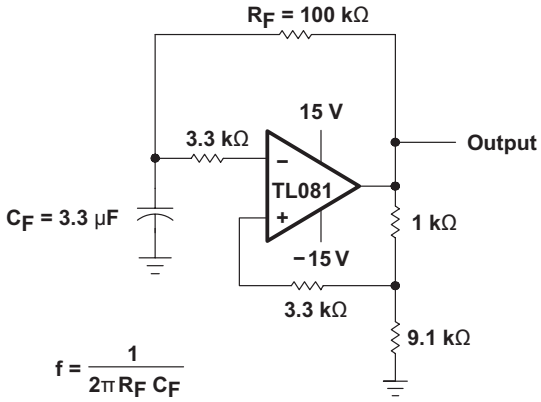



**Figure 25. 0.5-Hz Square-Wave Oscillator**

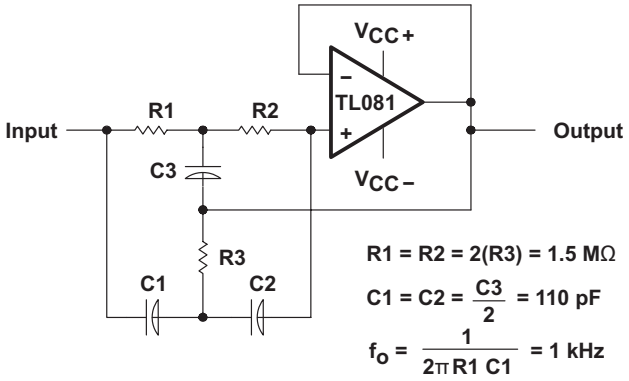



**Figure 26. High-Q Notch Filter**

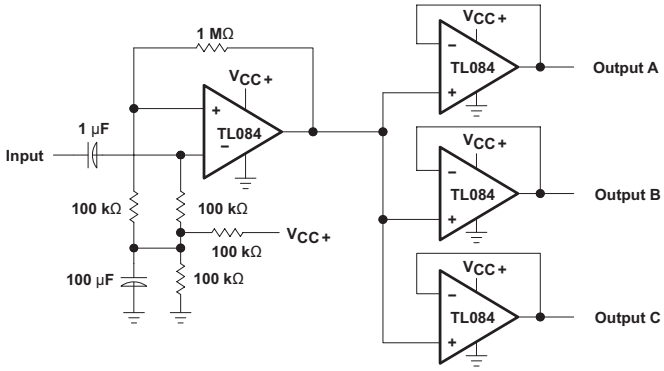
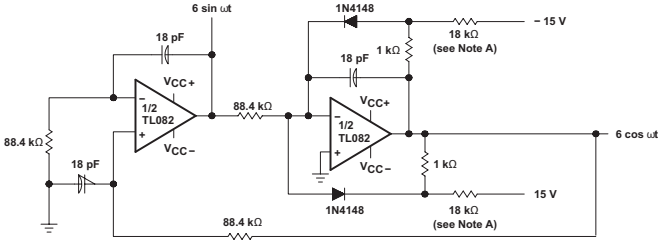



**Figure 27. Audio-Distribution Amplifier**




A. These resistor values may be adjusted for a symmetrical output.

**Figure 28. 100-kHz Quadrature Oscillator**

## System Examples (continued)

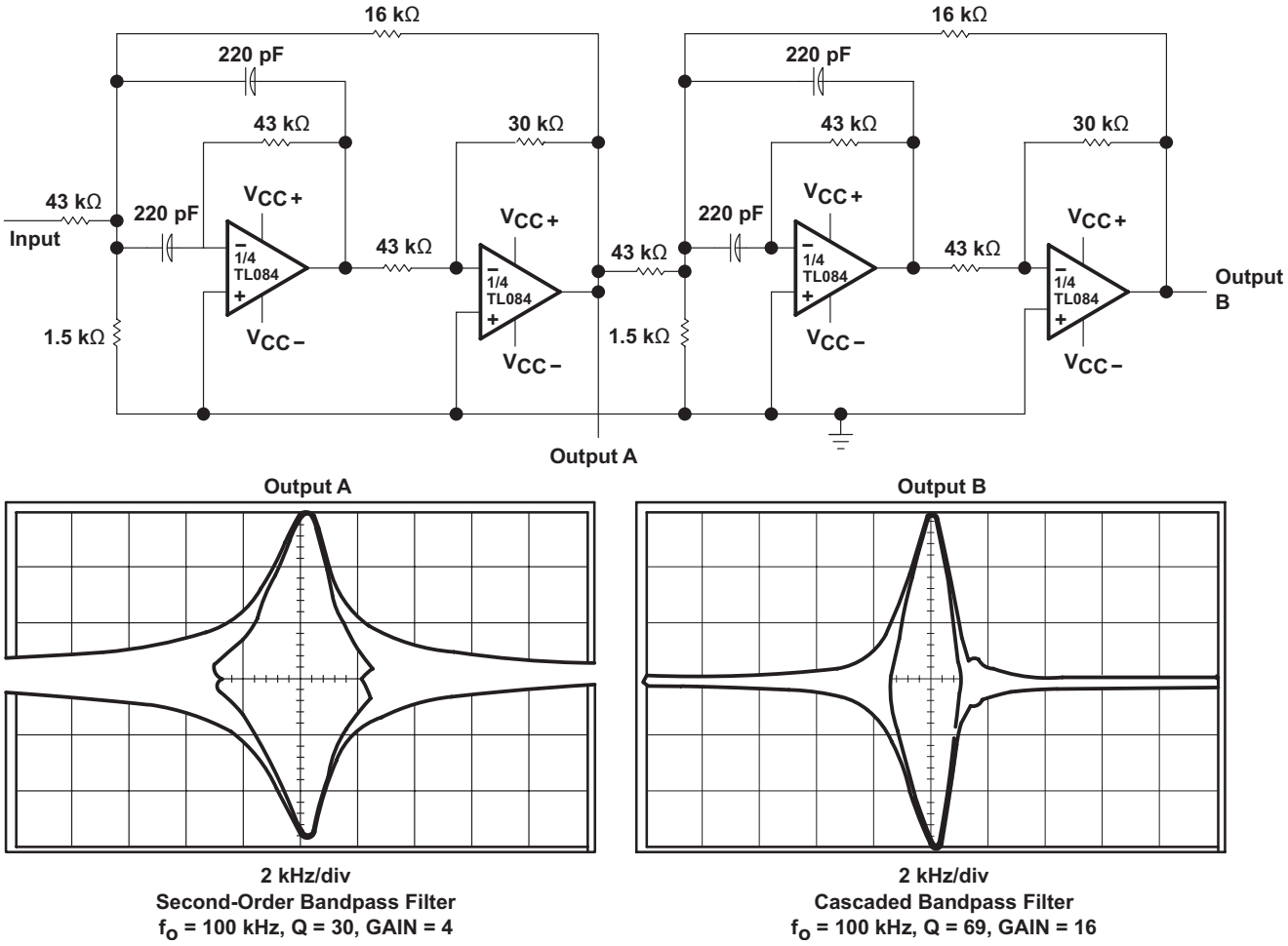



**Figure 29. Positive-Feedback Bandpass Filter**

# 10 Power Supply Recommendations

**CAUTION**

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see the *Absolute Maximum Ratings* ).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

# 11 Layout

## 11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Examples*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Examples

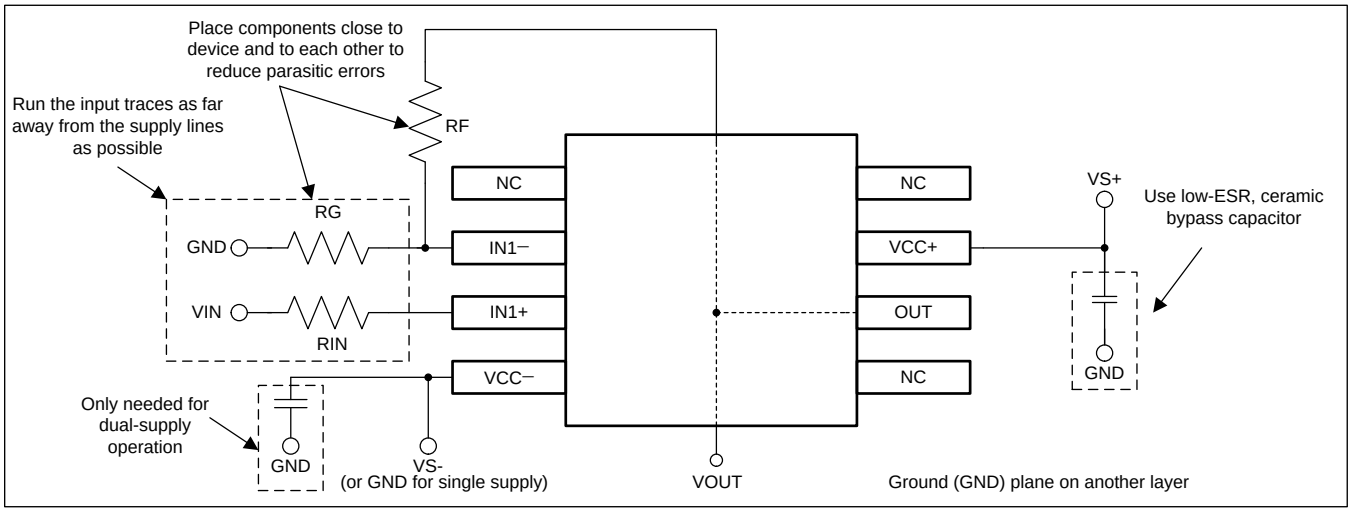



**Figure 30. Operational Amplifier Board Layout for Noninverting Configuration**

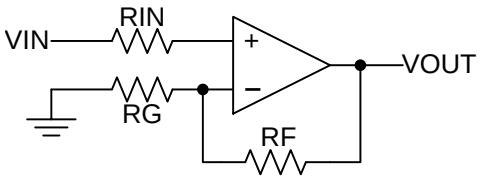



**Figure 31. Operational Amplifier Schematic for Noninverting Configuration**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For more information, see the following:

- *Circuit Board Layout Techniques*, SLOA089.

## 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| TL081 | Click here | Click here | Click here | Click here | Click here |
| TL081A | Click here | Click here | Click here | Click here | Click here |
| TL081B | Click here | Click here | Click here | Click here | Click here |
| TL082 | Click here | Click here | Click here | Click here | Click here |
| TL082A | Click here | Click here | Click here | Click here | Click here |
| TL082B | Click here | Click here | Click here | Click here | Click here |
| TL084 | Click here | Click here | Click here | Click here | Click here |
| TL084A | Click here | Click here | Click here | Click here | Click here |
| TL084B | Click here | Click here | Click here | Click here | Click here |

## 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9851501Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9851501Q2A TL082MFKB | Samples |
| 5962-9851501QPA | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9851501QPA TL082M | Samples |
| 5962-9851503Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9851503Q2A TL084 MFKB | Samples |
| 5962-9851503QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9851503QCA TL084MJB | Samples |
| TL081ACD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 081AC | Samples |
| TL081ACDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 081AC | Samples |
| TL081ACP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL081ACP | Samples |
| TL081BCD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 081BC | Samples |
| TL081BCDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 081BC | Samples |
| TL081BCP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL081BCP | Samples |
| TL081BCPE4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL081BCP | Samples |
| TL081CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL081C | Samples |
| TL081CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL081C | Samples |
| TL081CP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL081CP | Samples |
| TL081CPE4 | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL081CP | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL081CPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T081 | Samples |
| TL081ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL081I | Samples |
| TL081IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL081I | Samples |
| TL081IP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL081IP | Samples |
| TL082ACD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082AC | Samples |
| TL082ACDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082AC | Samples |
| TL082ACDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082AC | Samples |
| TL082ACDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082AC | Samples |
| TL082ACDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082AC | Samples |
| TL082ACDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082AC | Samples |
| TL082ACP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL082ACP | Samples |
| TL082ACPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T082A | Samples |
| TL082BCD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082BC | Samples |
| TL082BCDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082BC | Samples |
| TL082BCDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082BC | Samples |
| TL082BCDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082BC | Samples |
| TL082BCDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 082BC | Samples |
| TL082BCP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL082BCP | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL082BCPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL082BCP | Samples |
| TL082CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL082C | Samples |
| TL082CDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL082C | Samples |
| TL082CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL082C | Samples |
| TL082CDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL082C | Samples |
| TL082CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL082C | Samples |
| TL082CP | ACTIVE | PDIP | P | 8 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL082CP | Samples |
| TL082CPSR | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T082 | Samples |
| TL082CPSRG4 | ACTIVE | SO | PS | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T082 | Samples |
| TL082CPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T082 | Samples |
| TL082CPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T082 | Samples |
| TL082CPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T082 | Samples |
| TL082ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL082I | Samples |
| TL082IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL082I | Samples |
| TL082IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL082I | Samples |
| TL082IDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL082I | Samples |
| TL082IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL082I | Samples |
| TL082IP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL082IP | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL082IPE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL082IP | Samples |
| TL082IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | Z082 | Samples |
| TL082MFKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9851501Q2A TL082MFKB | Samples |
| TL082MJG | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | TL082MJG | Samples |
| TL082MJGB | ACTIVE | CDIP | JG | 8 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 9851501QPA TL082M | Samples |
| TL084ACD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084AC | Samples |
| TL084ACDE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084AC | Samples |
| TL084ACDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084AC | Samples |
| TL084ACDRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084AC | Samples |
| TL084ACDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084AC | Samples |
| TL084ACN | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL084ACN | Samples |
| TL084ACNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084A | Samples |
| TL084BCD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084BC | Samples |
| TL084BCDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084BC | Samples |
| TL084BCDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084BC | Samples |
| TL084BCN | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL084BCN | Samples |
| TL084BCNE4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL084BCN | Samples |
| TL084CD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084C | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL084CDE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084C | Samples |
| TL084CDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084C | Samples |
| TL084CDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084C | Samples |
| TL084CDRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084C | Samples |
| TL084CDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084C | Samples |
| TL084CN | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL084CN | Samples |
| TL084CNE4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | TL084CN | Samples |
| TL084CNSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL084 | Samples |
| TL084CPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T084 | Samples |
| TL084CPWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T084 | Samples |
| TL084CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T084 | Samples |
| TL084ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL084I | Samples |
| TL084IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL084I | Samples |
| TL084IDRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL084I | Samples |
| TL084IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL084I | Samples |
| TL084IN | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL084IN | Samples |
| TL084INE4 | ACTIVE | PDIP | N | 14 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | TL084IN | Samples |
| TL084MFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | TL084MFK | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TL084MFKB | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9851503Q2A TL084 MFKB | Samples |
| TL084MJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | TL084MJ | Samples |
| TL084MJB | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9851503QCA TL084MJB | Samples |
| TL084QD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL084Q | Samples |
| TL084QDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL084Q | Samples |
| TL084QDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL084Q | Samples |
| TL084QDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TL084Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF TL082, TL082M, TL084, TL084M :**

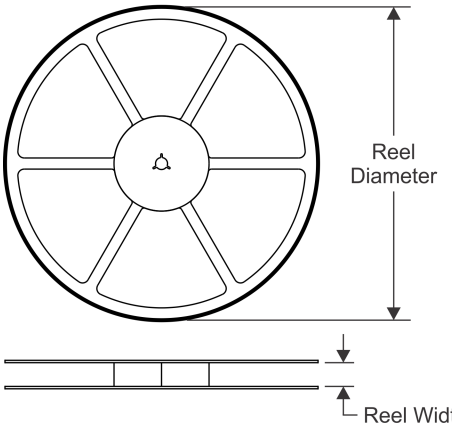
- Catalog: TL082, TL084
- Automotive: TL082-Q1, TL082-Q1
- Military: TL082M, TL084M

NOTE: Qualified Version Definitions:

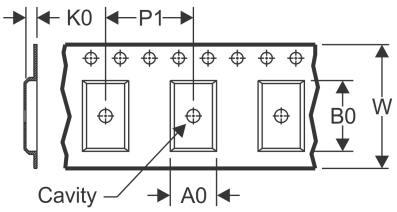
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

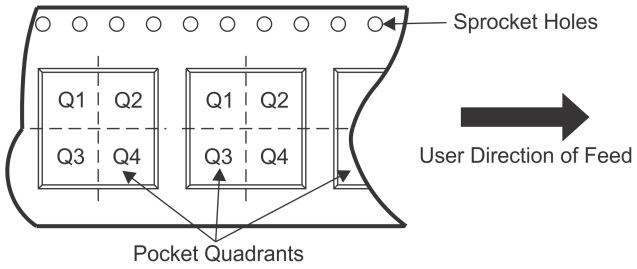



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

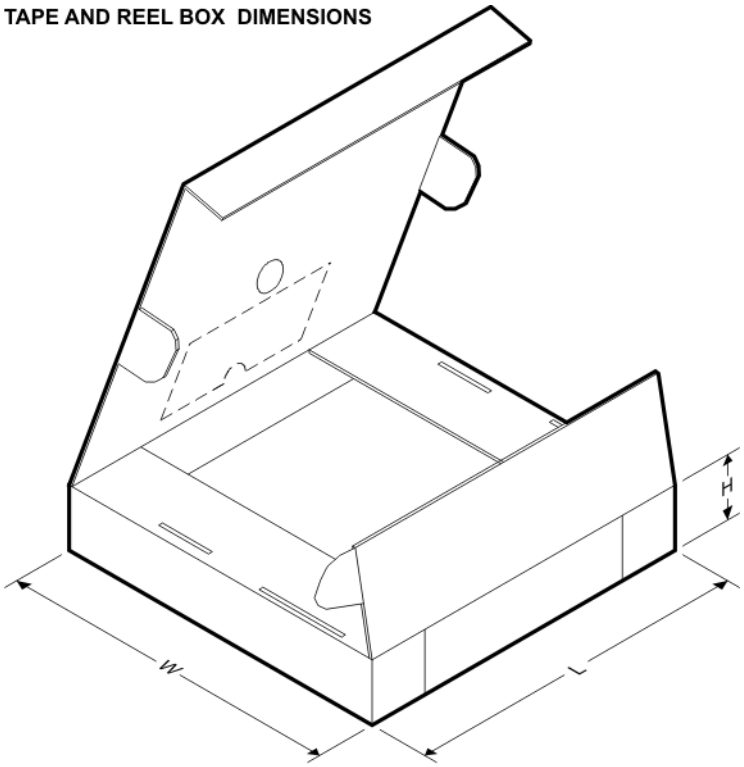



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL081ACDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL081BCDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL081CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL081CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| TL081IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082ACDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082ACDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082ACPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| TL082BCDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| TL082CPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL082IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL082IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL084ACDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL084ACDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL084ACNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TL084BCDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL084CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL084CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL084CDRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL084CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL084IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL084QDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL084QDRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



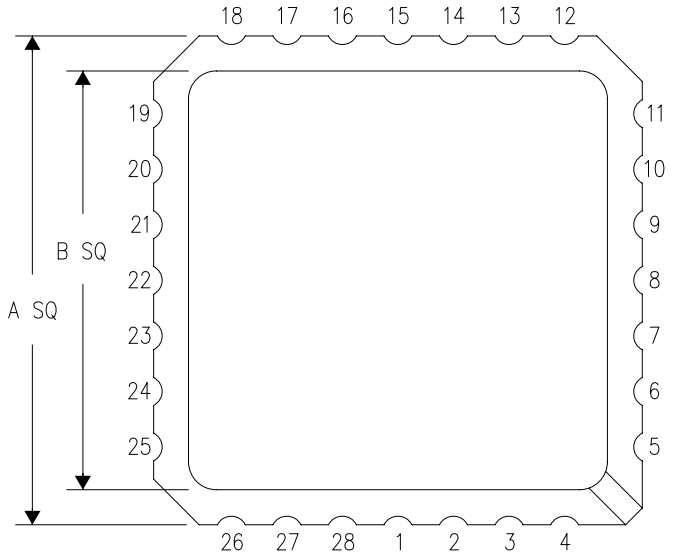

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL081ACDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL081BCDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL081CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL081CPSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |
| TL081IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL082ACDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TL082ACDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL082ACPSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |

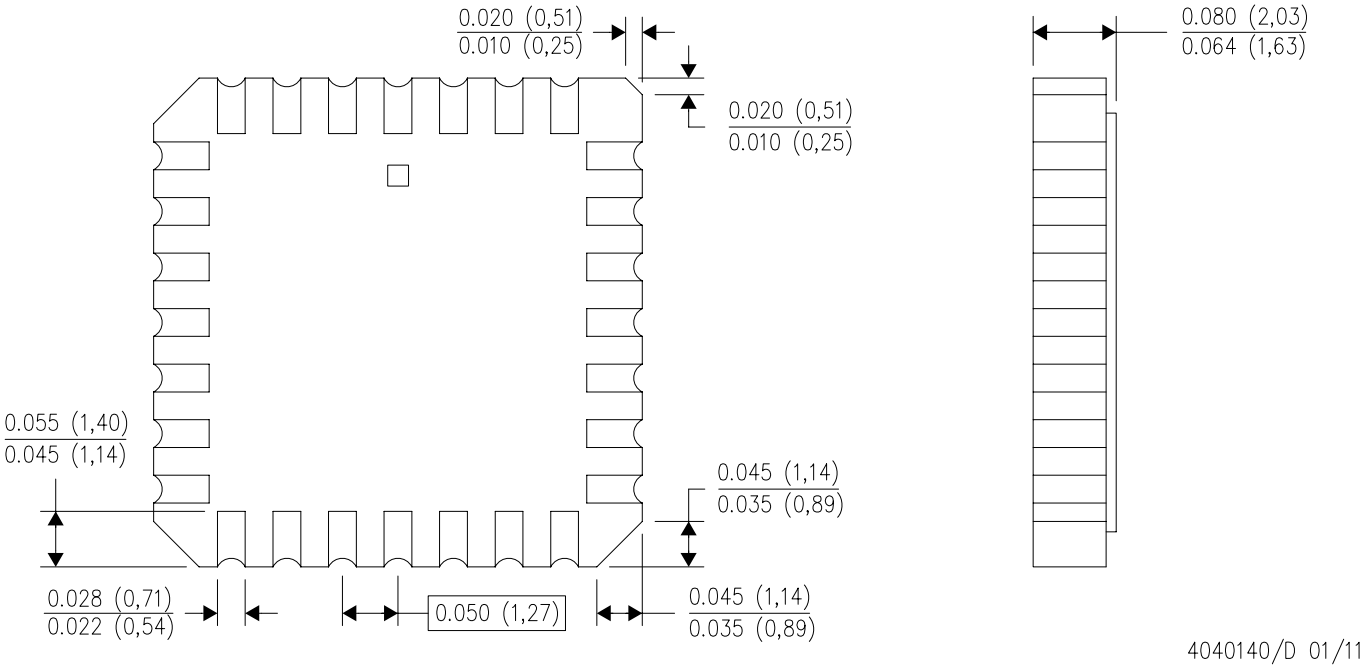
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL082BCDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL082CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL082CDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TL082CPSR | SO | PS | 8 | 2000 | 367.0 | 367.0 | 38.0 |
| TL082CPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TL082IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| TL082IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL082IPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |
| TL084ACDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL084ACDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL084ACNSR | SO | NS | 14 | 2000 | 367.0 | 367.0 | 38.0 |
| TL084BCDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL084CDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL084CDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL084CDRG4 | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL084CPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| TL084IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TL084QDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| TL084QDRG4 | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



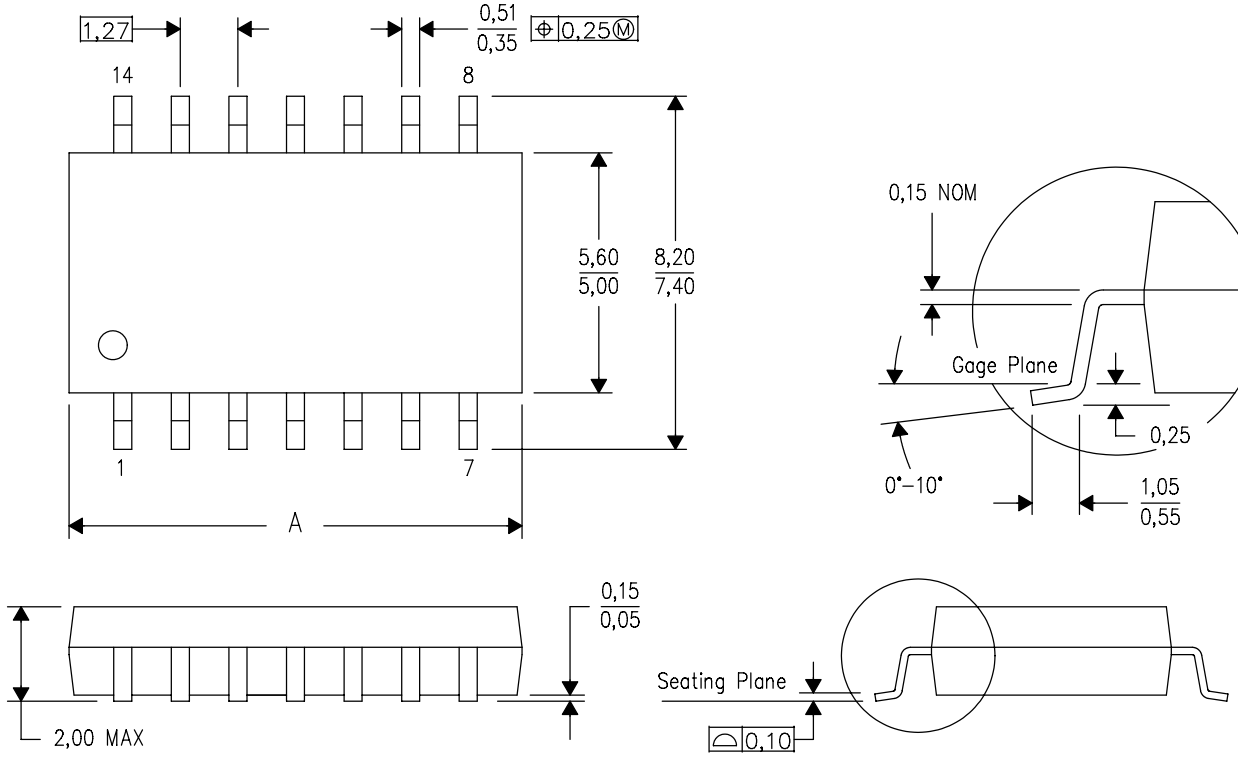

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

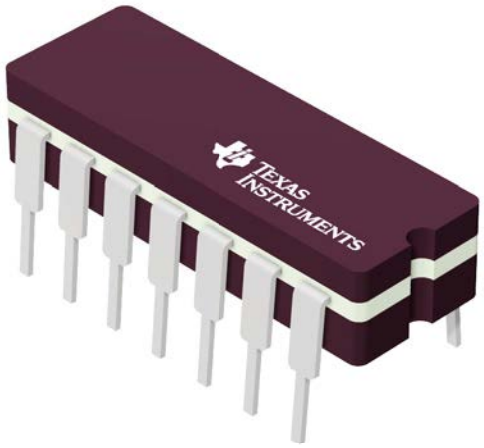
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

# GENERIC PACKAGE VIEW

## J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

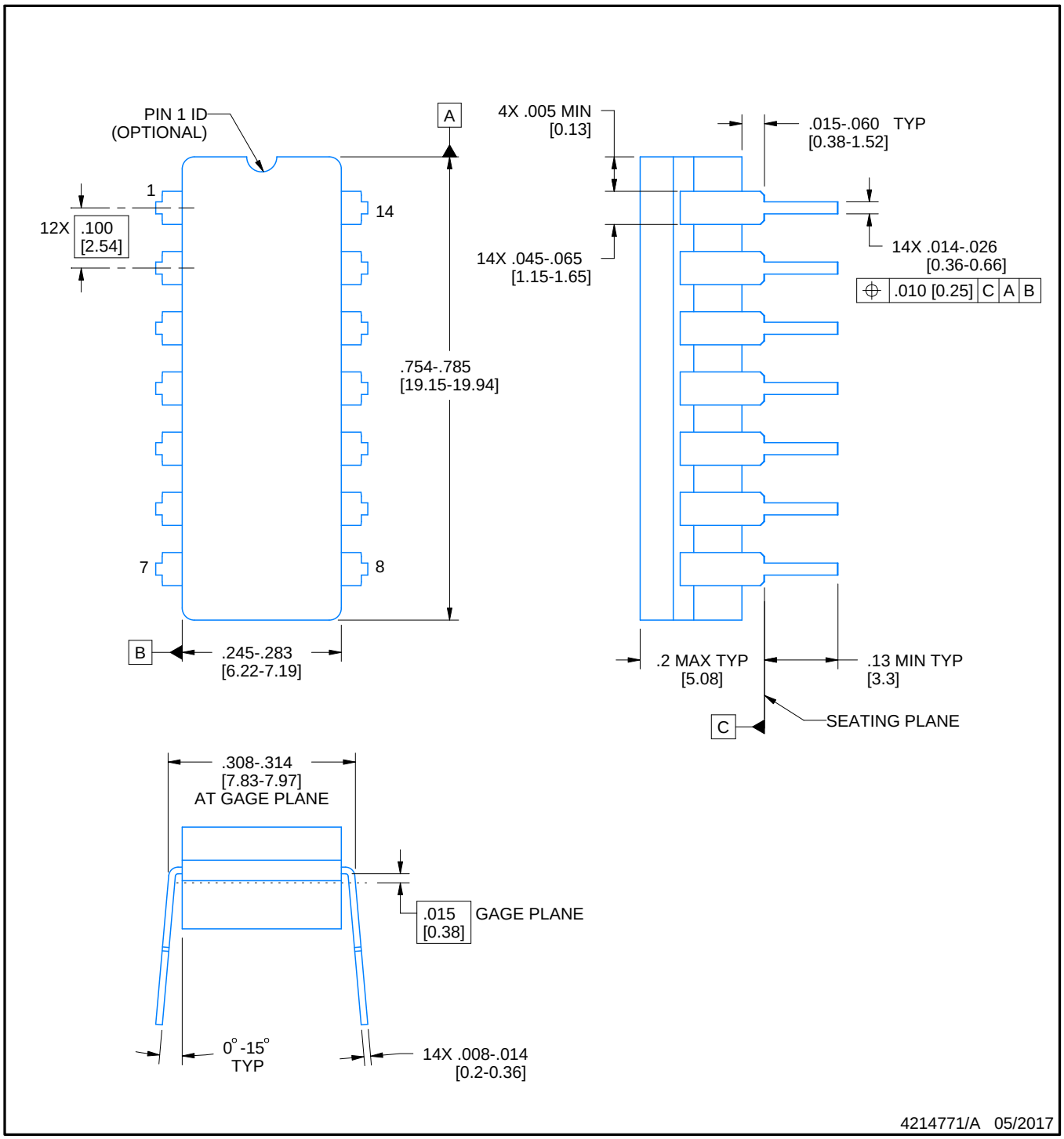
4040083-5/G

# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

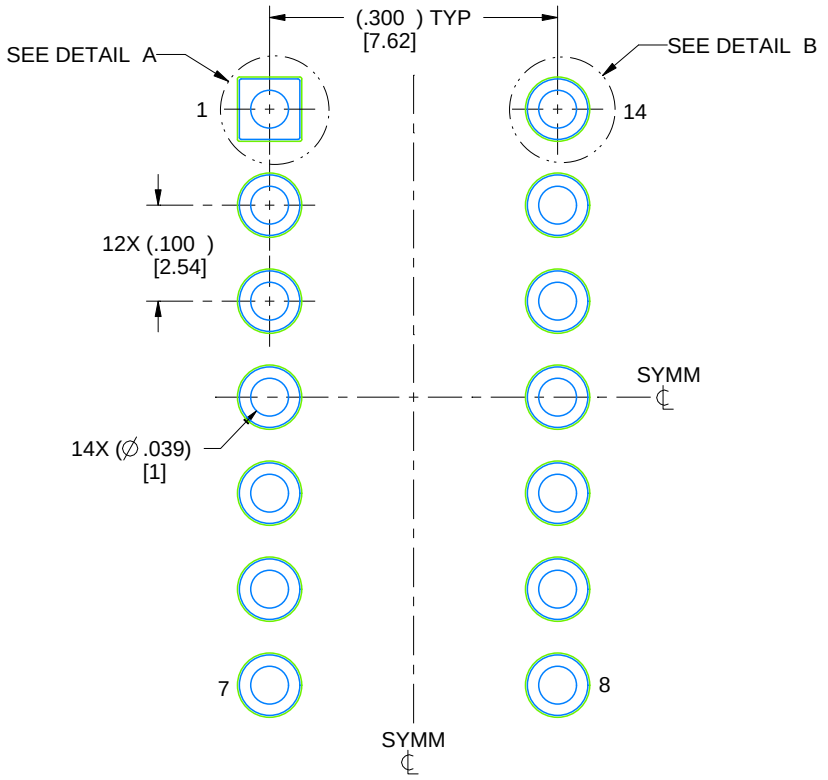
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

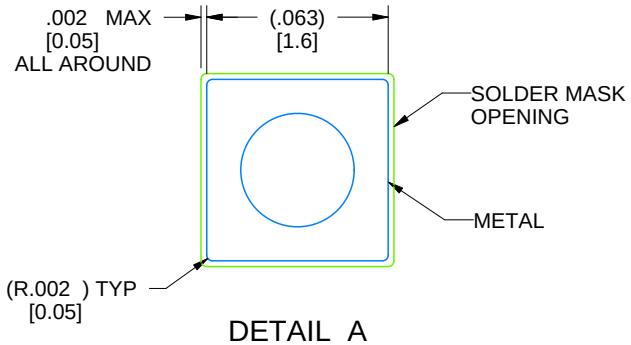
## J0014A

## CDIP - 5.08 mm max height

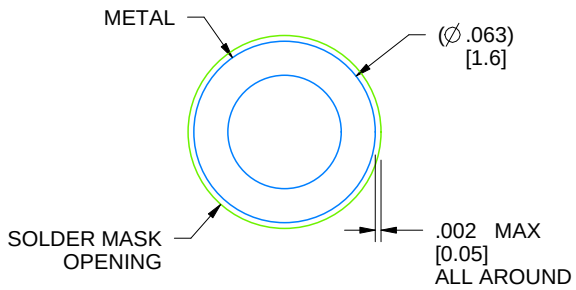
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



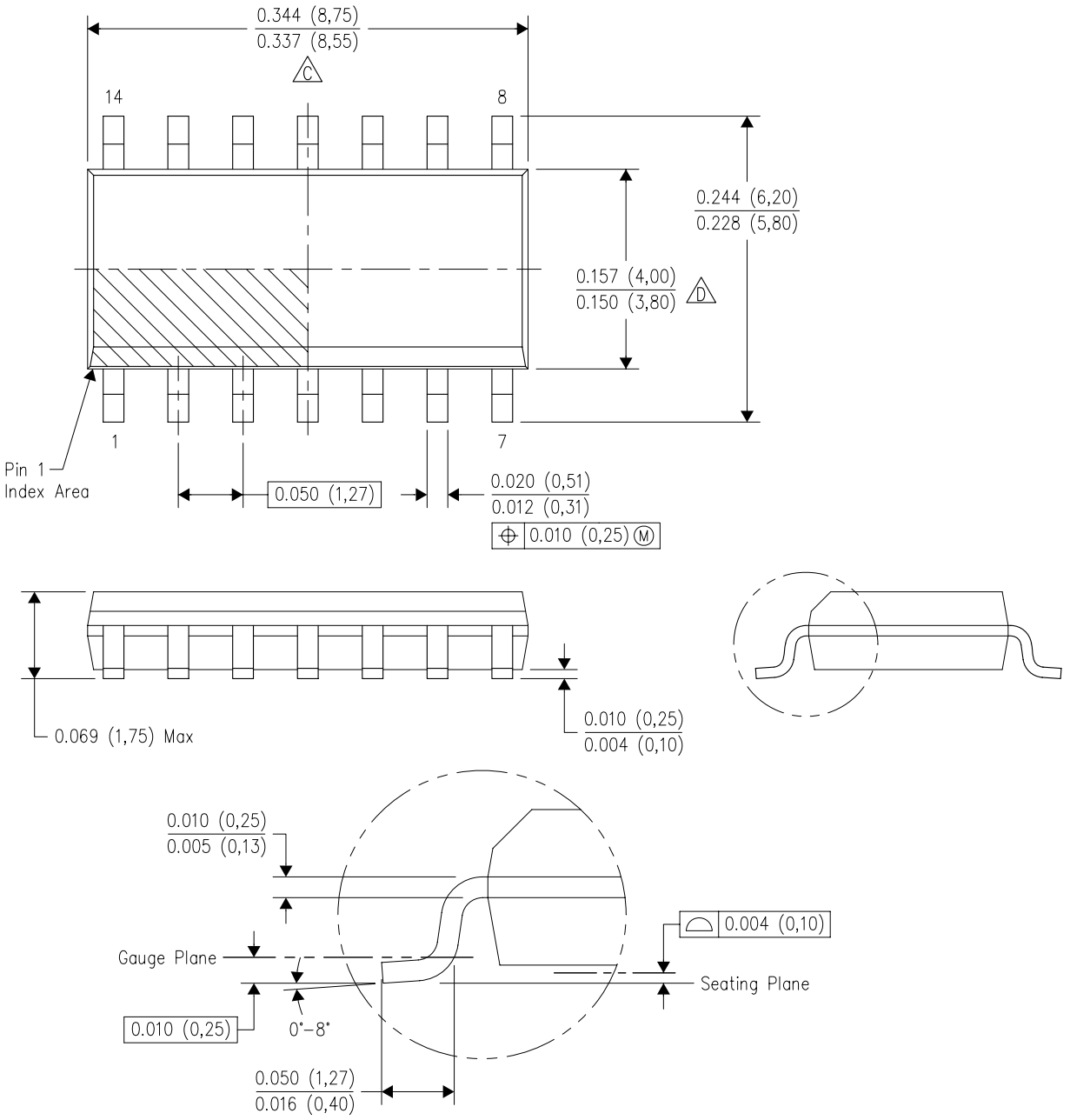

DETAIL A
SCALE: 15X




DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

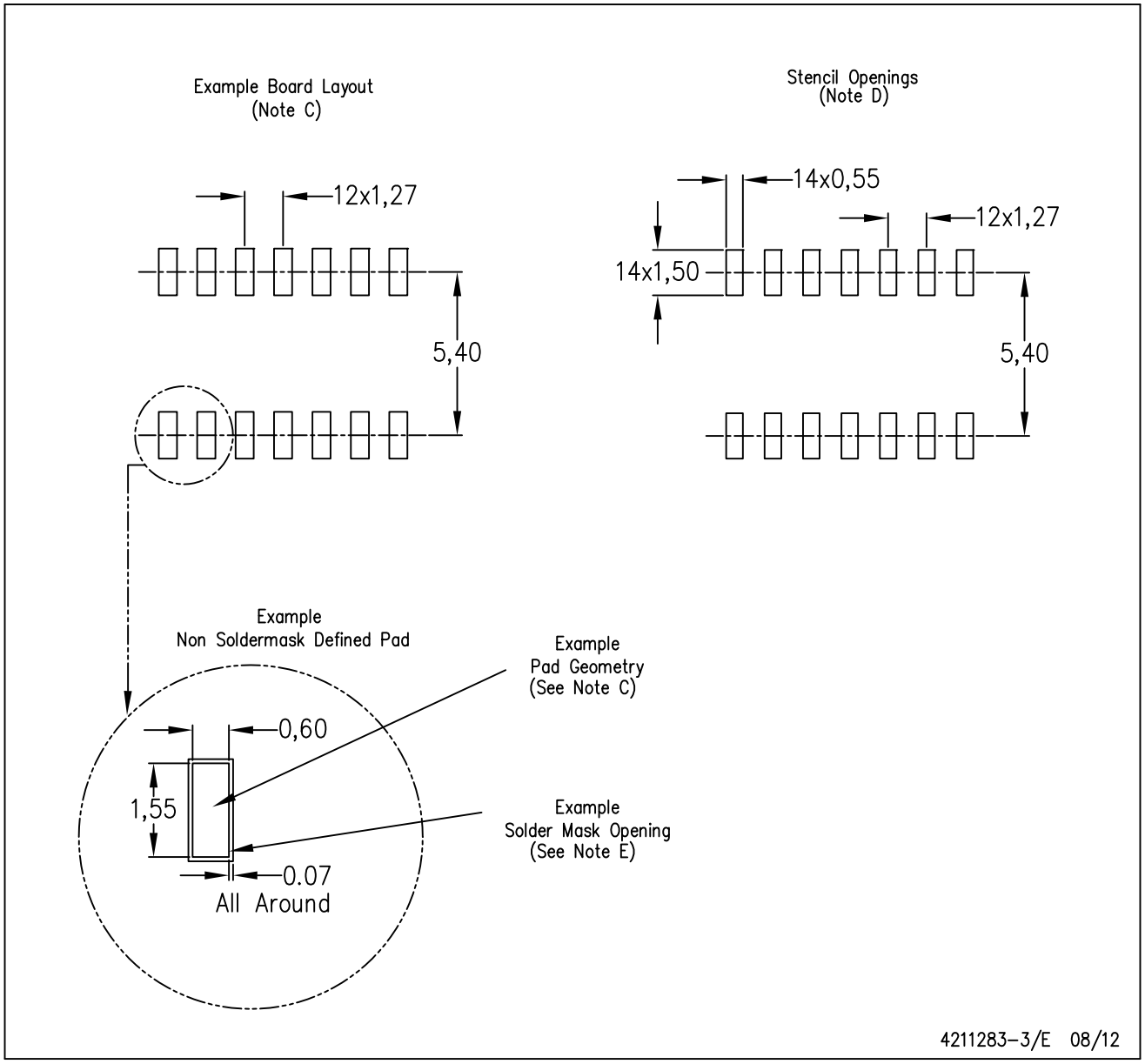
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040047–5/M 06/11

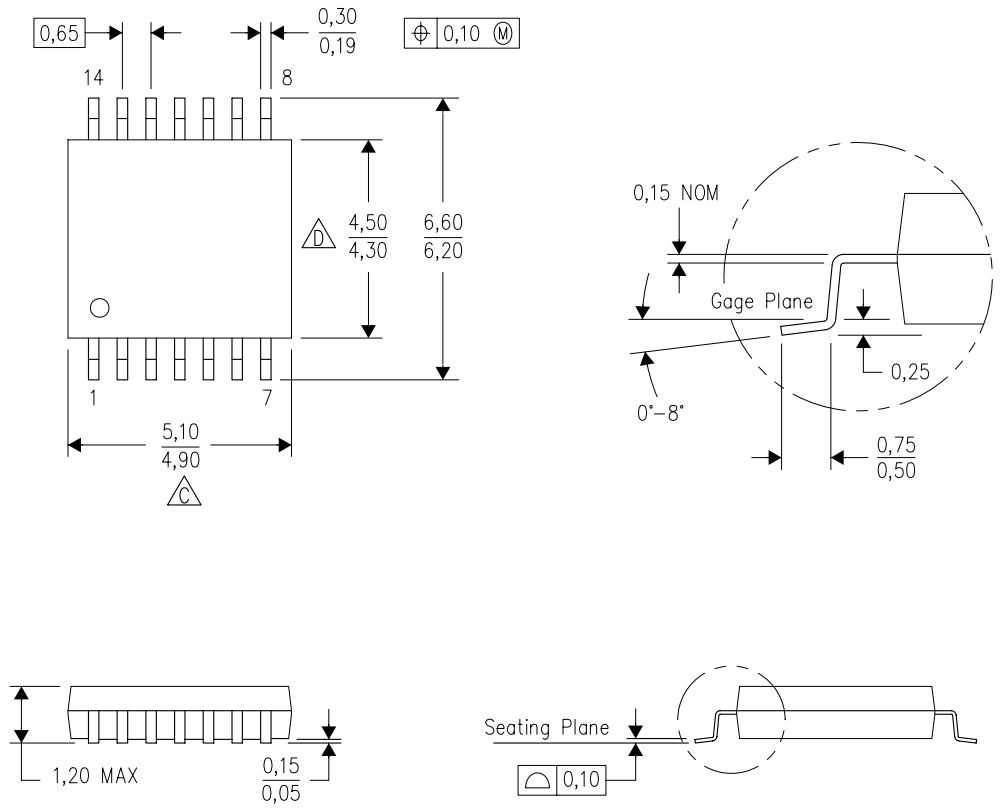
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

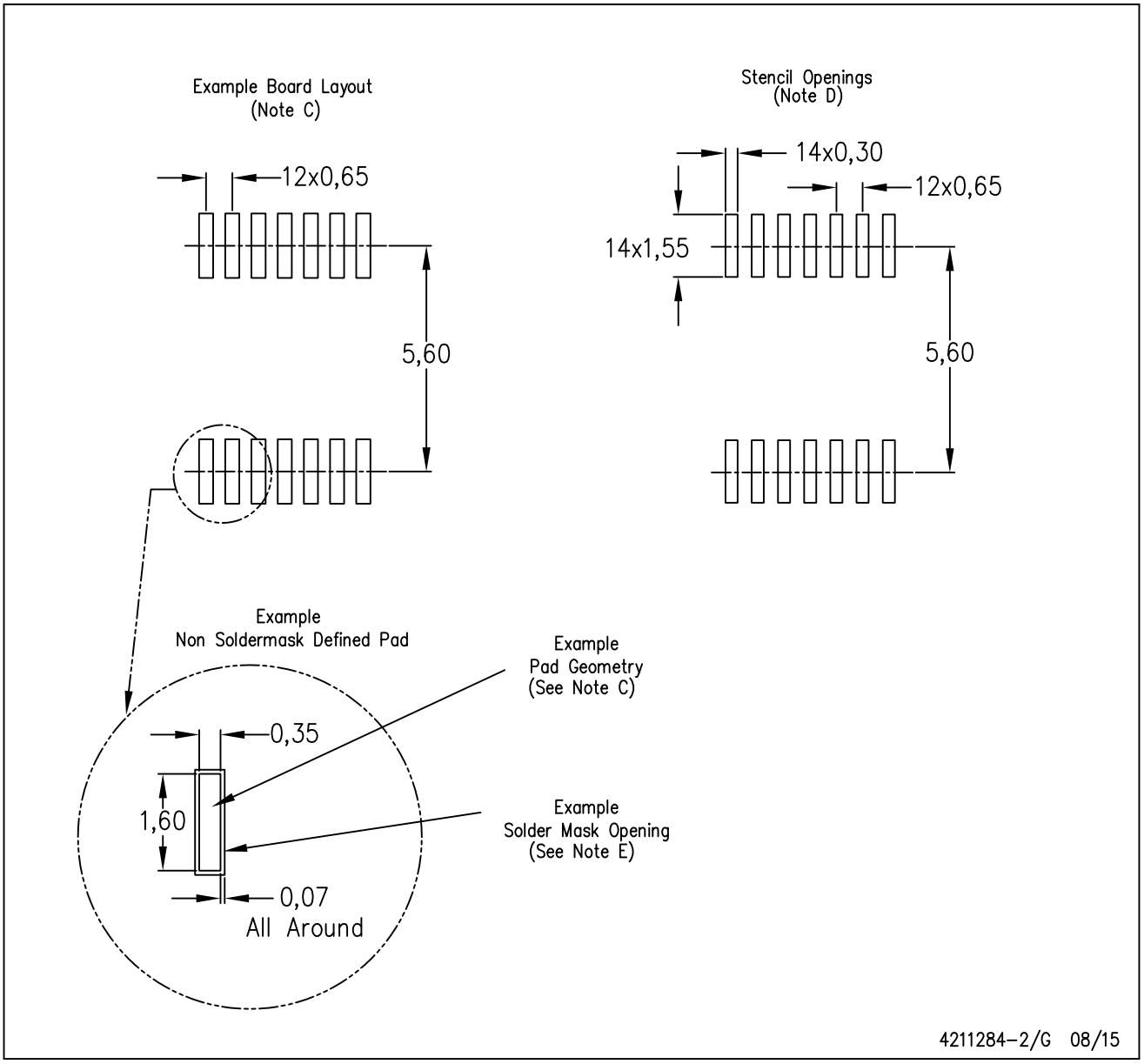
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

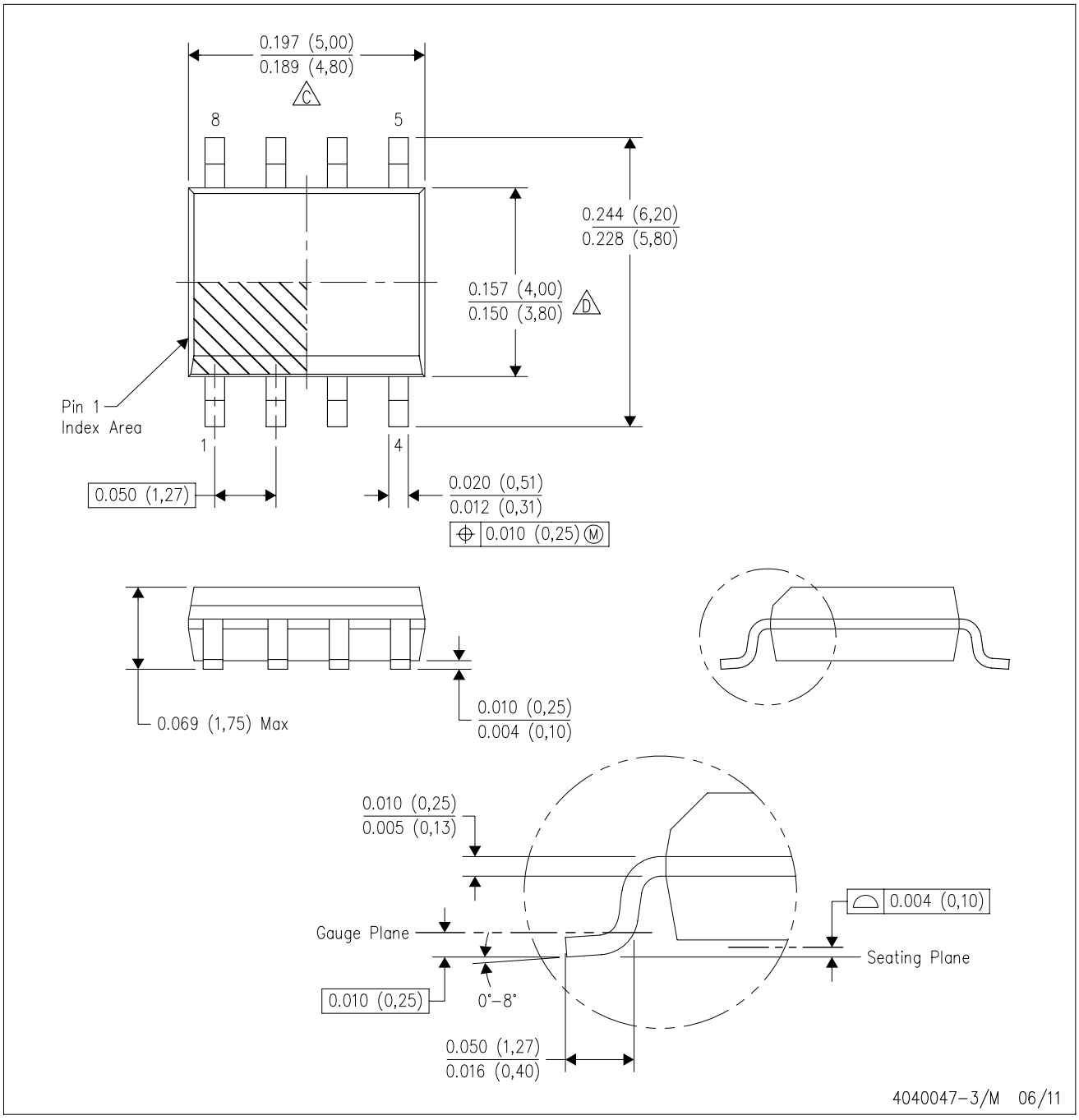
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



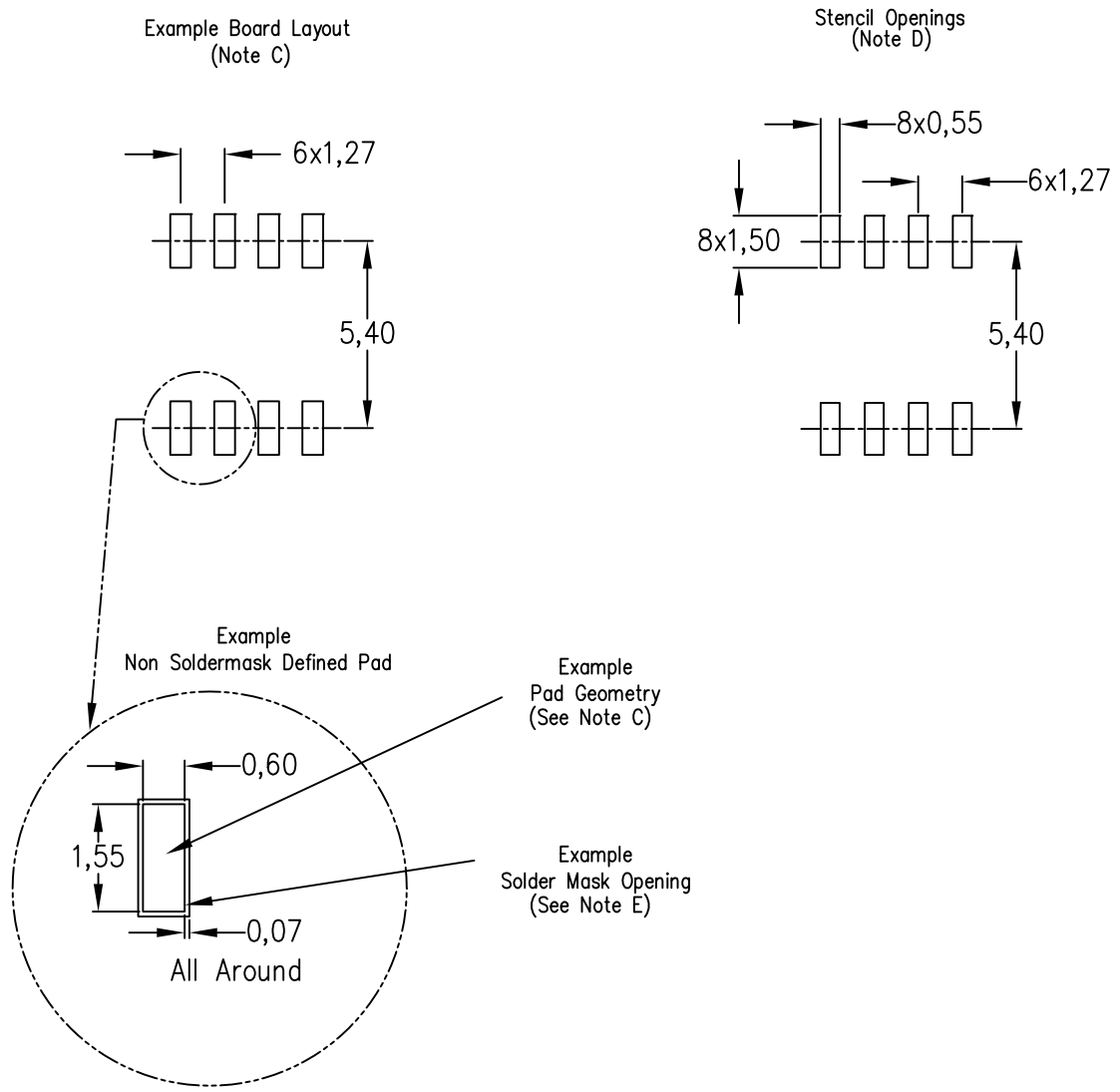

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

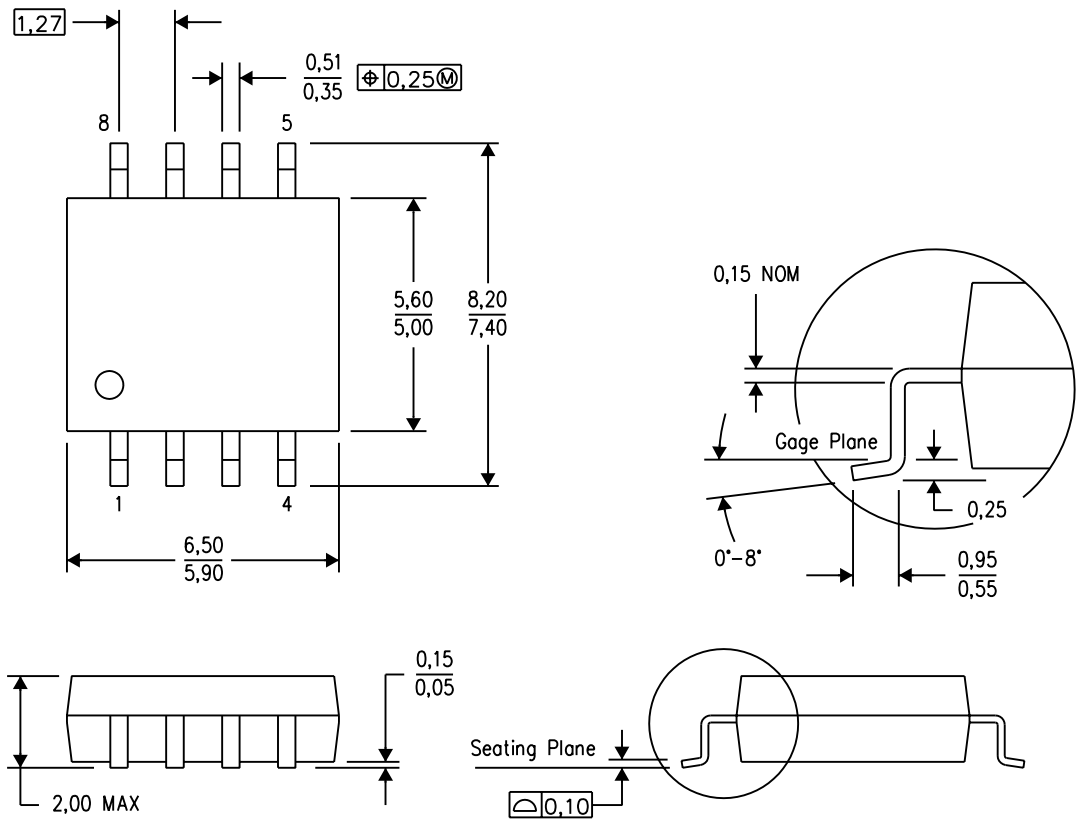
D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

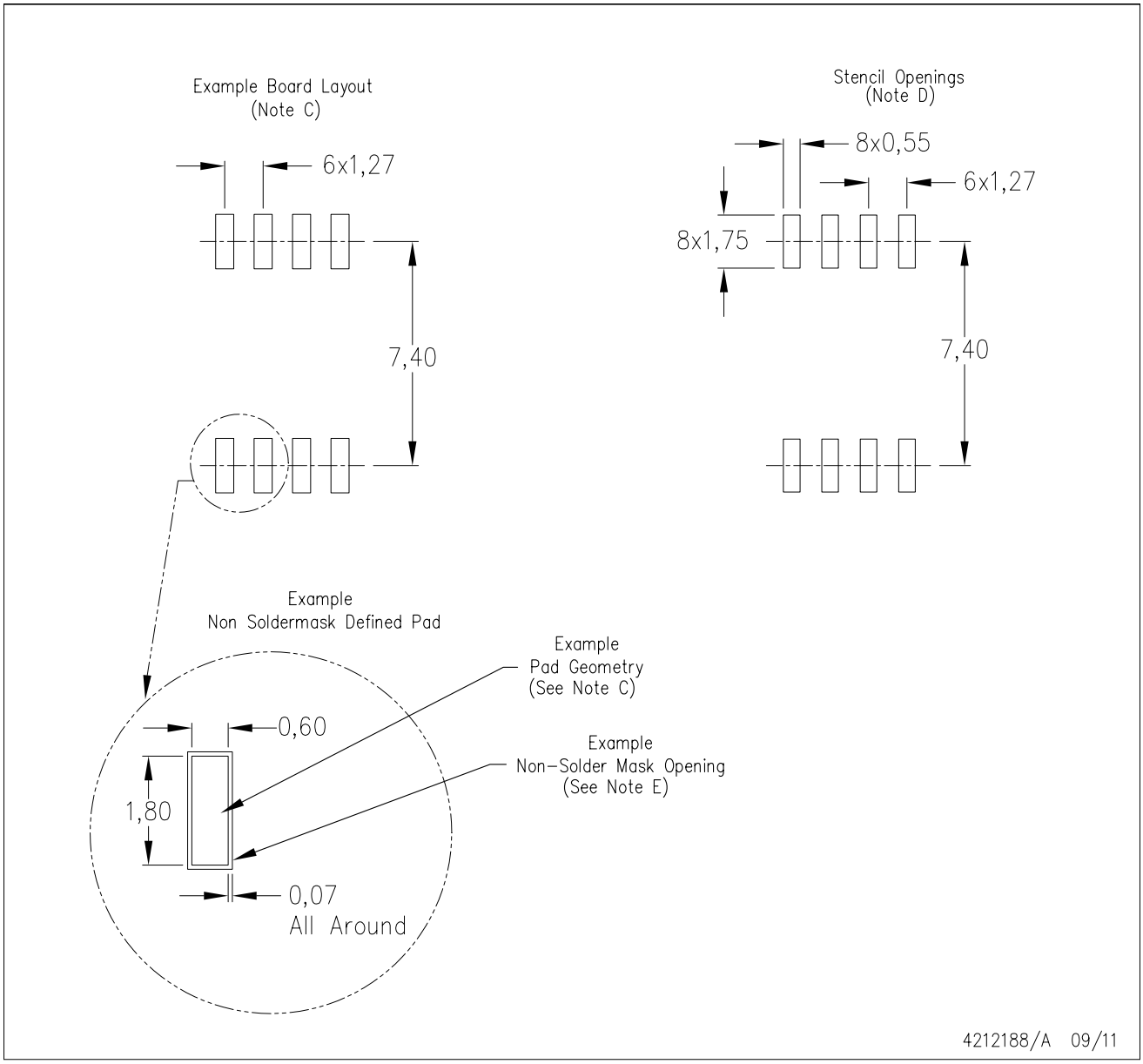
**PS (R-PDSO-G8)** **PLASTIC SMALL-OUTLINE PACKAGE**




4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

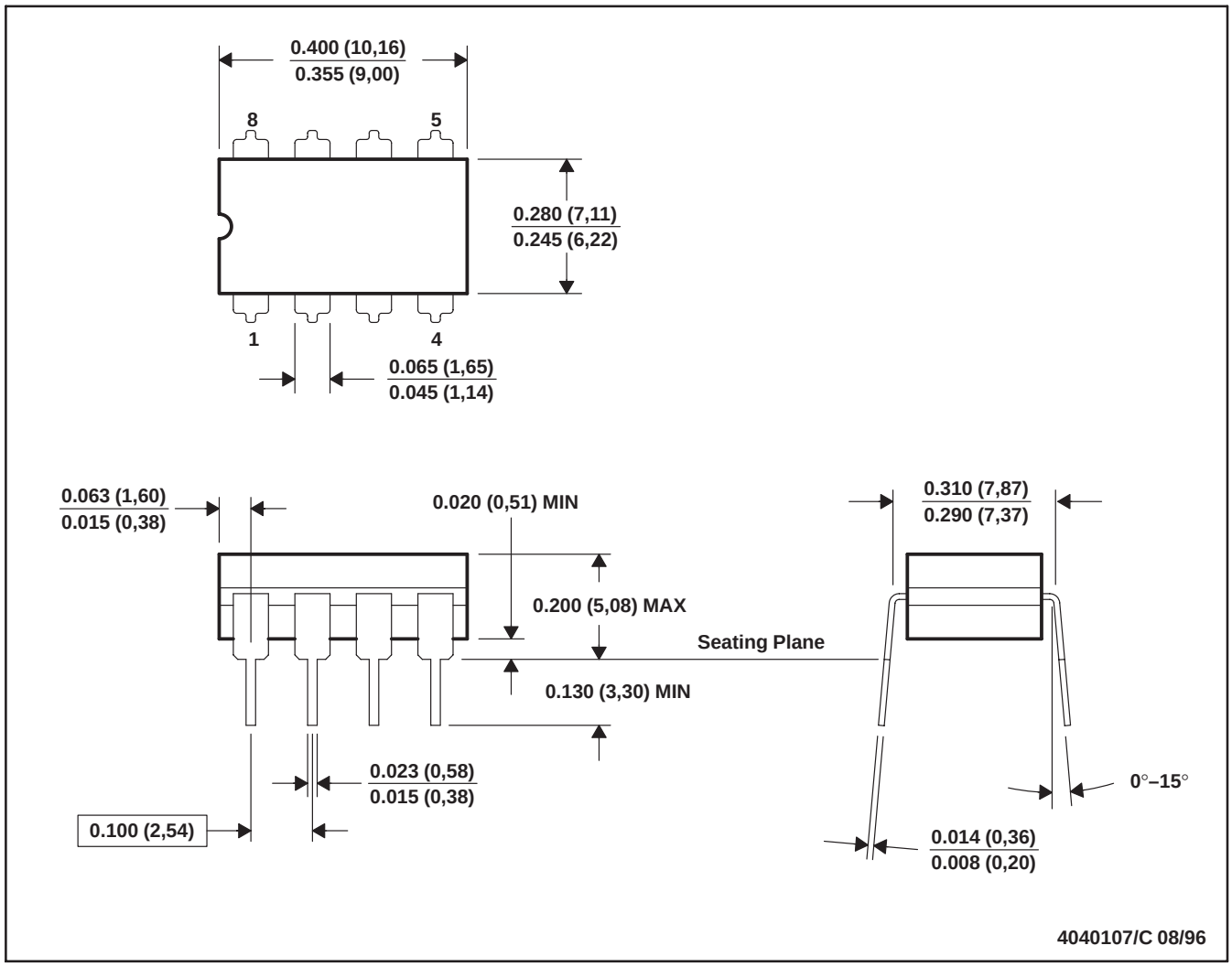
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

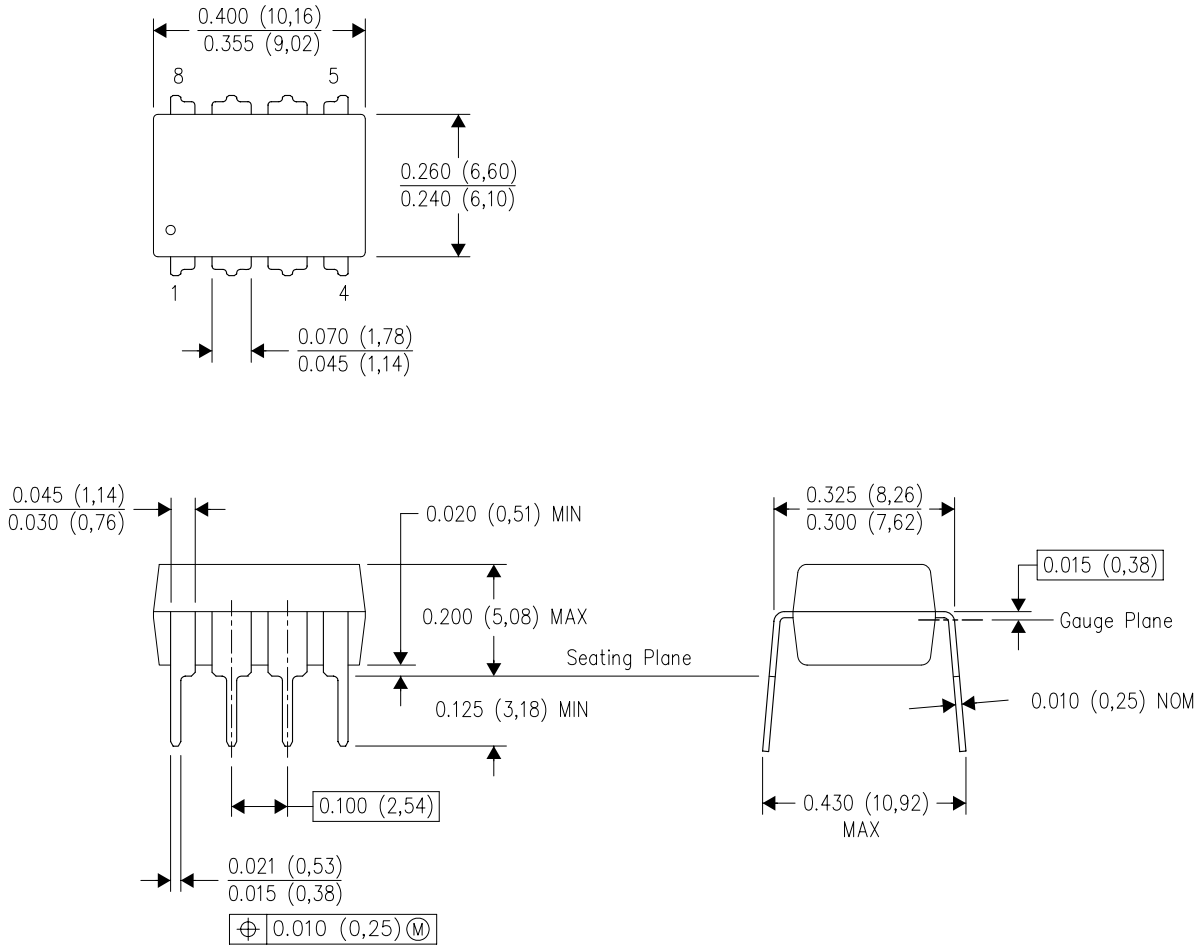
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

**JG (R-GDIP-T8)** **CERAMIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

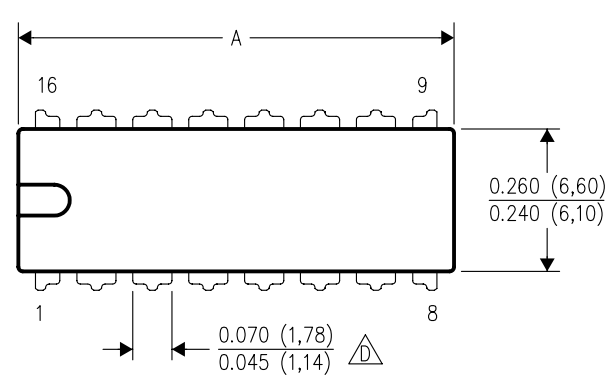



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

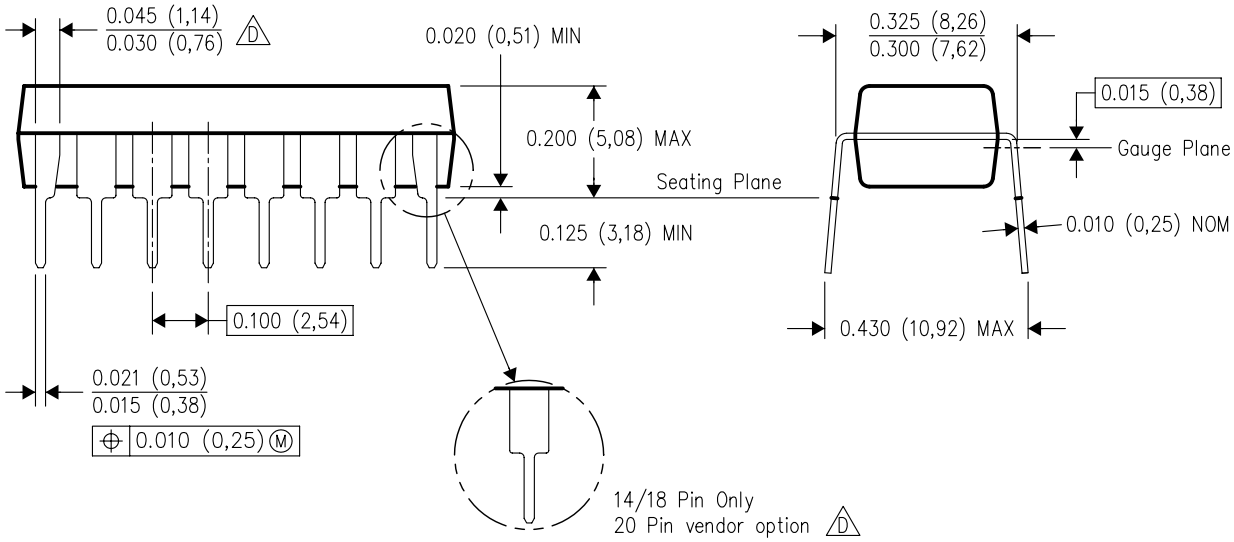
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

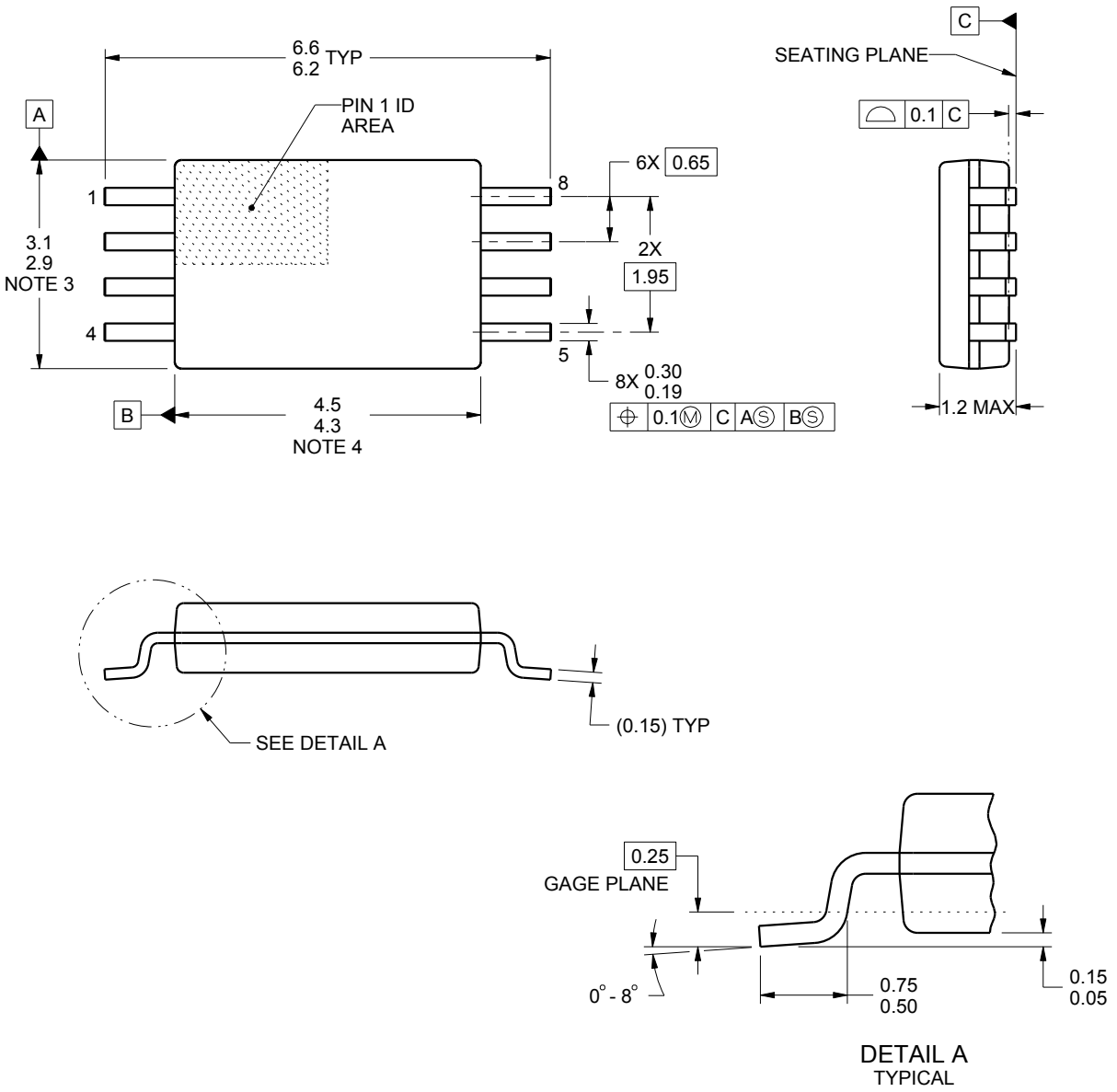
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## PW0008A

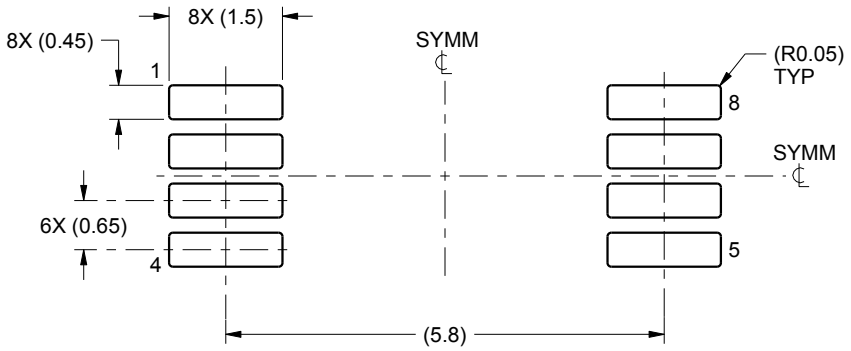
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

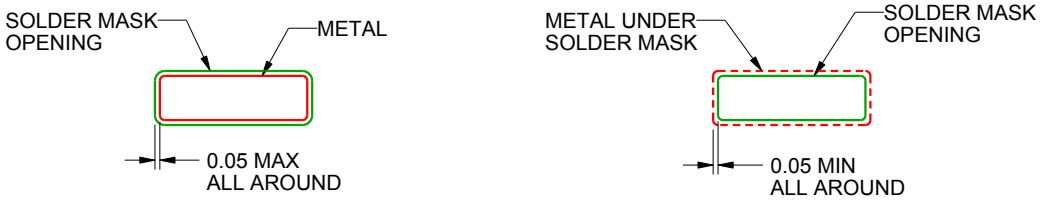



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.




LAND PATTERN EXAMPLE
SCALE:10X

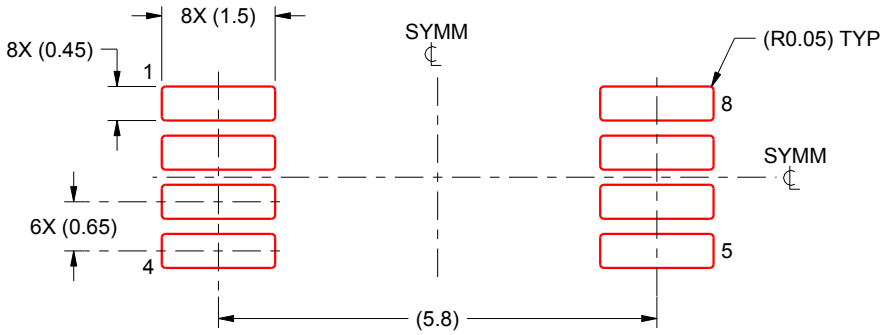



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Tema n. 2

Nell’ambito dei dispositivi M/NEMS (Micro/Nano Electro Mechanical System) è possibile identificare i sistemi per le applicazioni biologiche come componenti che stanno avendo un notevole incremento di interesse.

Il candidato, basandosi su una o più delle metodologie tipiche della tecnologia M/NEMS, progetti una struttura per la realizzazione di un dispositivo da utilizzare come sensore di batteri patogeni o virus.

In particolare:

- si riporti uno schematico del dispositivo;
- si descriva il flusso dei passi di processo inquadrandolo nella tecnologia di fabbricazione scelta.

Viene richiesto inoltre di affrontare il problema del packaging del dispositivo e l’integrazione con l’elettronica di gestione.

È necessaria una trattazione con scelte motivate, precise, schematiche e quantitative.

Tema n. 3

Si progetti un sistema di comunicazione su fibra ottica a lunga distanza e alta capacità per stabilire un collegamento tra due punti fissi atto alla trasmissione di flussi di informazione digitale.

La capacità complessiva per fibra del sistema deve essere di 5 Tbit/s.
Sono inoltre dati i seguenti vincoli del sistema:

- Distanza: 2000 km;
- Tipo di fibra: singolo modo SMF G.652;
- Amplificatori ottici di tipo EDFA.

Per i parametri fisici del collegamento si assumano valori tipici motivandone la scelta.

Sulla base di queste assunzioni, si dimensionino i principali parametri del sistema di trasmissione in modo da garantire la capacità richiesta con i vincoli posti.

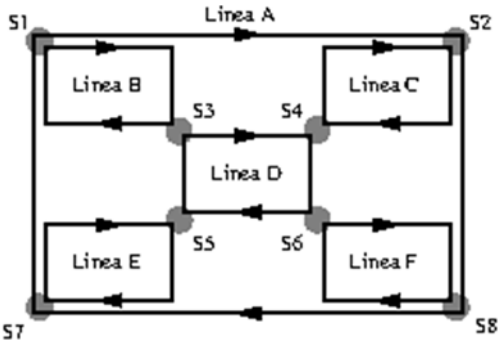
In particolare:

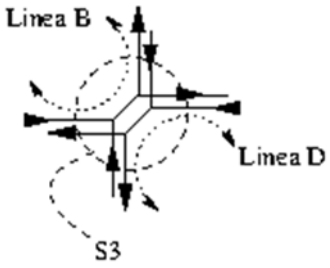
- si determini il formato di modulazione, il tipo di multiplazione, i livelli di potenza e ogni altro parametro relativo ai transceiver che dovranno essere utilizzati;
- si determini il piano delle lunghezze d'onda utilizzate;
- si determini le caratteristiche e il posizionamento degli EDFA;
- si discuta quali sono gli effetti propagativi limitanti il sistema e si specifichi quali sono stati considerati nella progettazione del sistema.

Terminato il progetto si commenti sulla possibilità di possibili futuri aggiornamenti e miglioramenti del sistema per aumentarne la capacità complessiva per fibra: si indichino quali potrebbero essere le strategie possibili stimando l'entità dell'incremento di capacità.

Tema n. 4

Si desidera creare una applicazione in grado di simulare e controllare una piccola rete metropolitana.
La struttura semplificata di tale rete è rappresentata dalla seguente immagine:




Come indicato dall'immagine di sinistra, la rete è costituita da 6 linee di metropolitana (Linea A – Linea F, di forma rettangolare e colore nero) e da 8 stazioni (S1 – S8, di forma circolare e colore grigio).
Ogni linea prevede entrambi i sensi di percorrenza (orario e anti-orario). Ogni stazione è in comune a due linee di metropolitana. I binari di tutte le linee sono doppi (una linea ferrata per ogni direzione di marcia), ma in ogni stazione ogni coppia di binari è in comune a due linee ferroviarie, come rappresentato nell'immagine di destra per la stazione S3. Dato questo vincolo, in ogni stazione può accedere un solo convoglio alla volta per ciascun senso di marcia. Il convoglio successivo può entrarvi solo quando quello precedente vi è uscito. Convogli provenienti da linee metropolitane diverse che vogliano accedere contestualmente alla stessa stazione lo possono fare seguendo una strategia FIFO.

Oltre ai limiti strutturali sopracitati, la metropolitana deve rispettare i seguenti vincoli:

- Tutti i convogli che viaggiano sulla metropolitana sono identici e possono contenere al massimo 100 passeggeri. Ogni convoglio
  - Impiega $T_{Tragitto}$ secondi per spostarsi da una stazione all'altra (valore predefinito e costante per tutte le tratte)
  - Si ferma $T_{stop}$ secondi in ogni stazione, con
    - $T_{stop} = \alpha \cdot (N_{in} + N_{out})$

    dove $\alpha$ è un numero casuale incluso nell'intervallo ]0, 1], $N_{in}$ è il numero di passeggeri che salgono nel convoglio e $N_{out}$ il numero di passeggeri che scendono.
- Il numero di passeggeri che desiderano salire su (oppure scendere da) un convoglio si suppone noto nel momento in cui ogni convoglio stesso entra in una stazione (e differisce ovviamente per ciascun convoglio e ciascuna stazione). A livello di simulazione si produca tale effetto utilizzando la generazione di un numero casuale compreso nell'intervallo che va da 0 a 200 per i passeggeri che vogliono salire e da 0 al numero passeggeri sul convoglio per quelli che devono scendere. Si osservi inoltre che il numero di passeggeri che possono effettivamente salire su ciascun convoglio è limitato dal numero di posti liberi sul convoglio stesso e che i passeggeri che non riescono a salire su un convoglio devono attendere il successivo.
- Il numero di convogli in marcia in ciascuna direzione viene regolato automaticamente in ciascuna stazione seguendo le regole successive:

- Quando l'applicazione viene eseguita, nessun convoglio è in marcia.
- Un nuovo convoglio viene attivato ogni volta che il numero di passeggeri in attesa (su quella linea e in quella direzione) è superiore a 50 per un tempo superiore a quello che corrispondente al passaggio di tre convogli successivi.
- Se il numero di passeggeri in attesa di un convoglio è inferiore a 20 per un tempo superiore a quello che corrispondente al passaggio di tre convogli successivi, il convoglio successivo viene soppresso facendo scendere in stazione tutti i passeggeri.

Si sviluppi, in ambiente UNIX/Linux oppure Windows e il linguaggio C-like, una applicazione in grado di simulare la rete metropolitana indicata. In particolare l'applicazione deve essere in grado di:

- Rappresentare ciascuna stazione mediante un thread.
- Rappresentare ciascun convoglio mediante un thread.
- Gestire un numero di passeggeri casuale in ingresso e in uscita di ciascun convoglio in ciascuna direzione di marcia di ciascuna linea.
- Simulare dinamicamente l'aumento e la diminuzione del numero di convogli (thread) circolanti su ciascuna linea.
- Interrompere il servizio su una linea quando tutti i convogli sono fuori servizio (a causa di un numero di passeggeri troppo esiguo).
- Riprendere il servizio su una linea quando il numero di passeggeri in stazione prevede la creazione di un nuovo convoglio.

L'applicazione visualizzi (a video) una sequenza di messaggi che indichino il susseguirsi delle azioni verificatesi in metropolitana, per esempio:

```
stazione=1  linea=A  direzione=oraria creatoConvoglio=1
stazione=1  linea=A  convoglio=1  passeggeriIn=40  passeggeriOut=0
stazione=1  linea=B  direzione=oraria creatoConvoglio=2
stazione=1  linea=B  convoglio=2  passeggeriIn=38  passeggeriOut=0
stazione=2  linea=A  convoglio=1  passeggeriIn=23  passeggeriOut=12
stazione=6  linea=F  direzione=antioraria creatoConvoglio=3
stazione=6  linea=F  convoglio=3  passeggeriIn=59  passeggeriOut=0
…
```

Si indichi inoltre come sia possibile simulare correttamente:

- la gestione di avvenimenti imprevisti, quali ad esempio il guasto di un convoglio che deve quindi essere sostituito con trasbordo dei passeggeri;
- la saturazione della rete ferroviaria a causa di un eccessivo numero di utenti e/o convogli su una o più linee.